

KSWAA/KTWAA

Liverpool 10M/10MG

Sunderland 10M/10MG

LA-4982P REV 1.0 Schematic

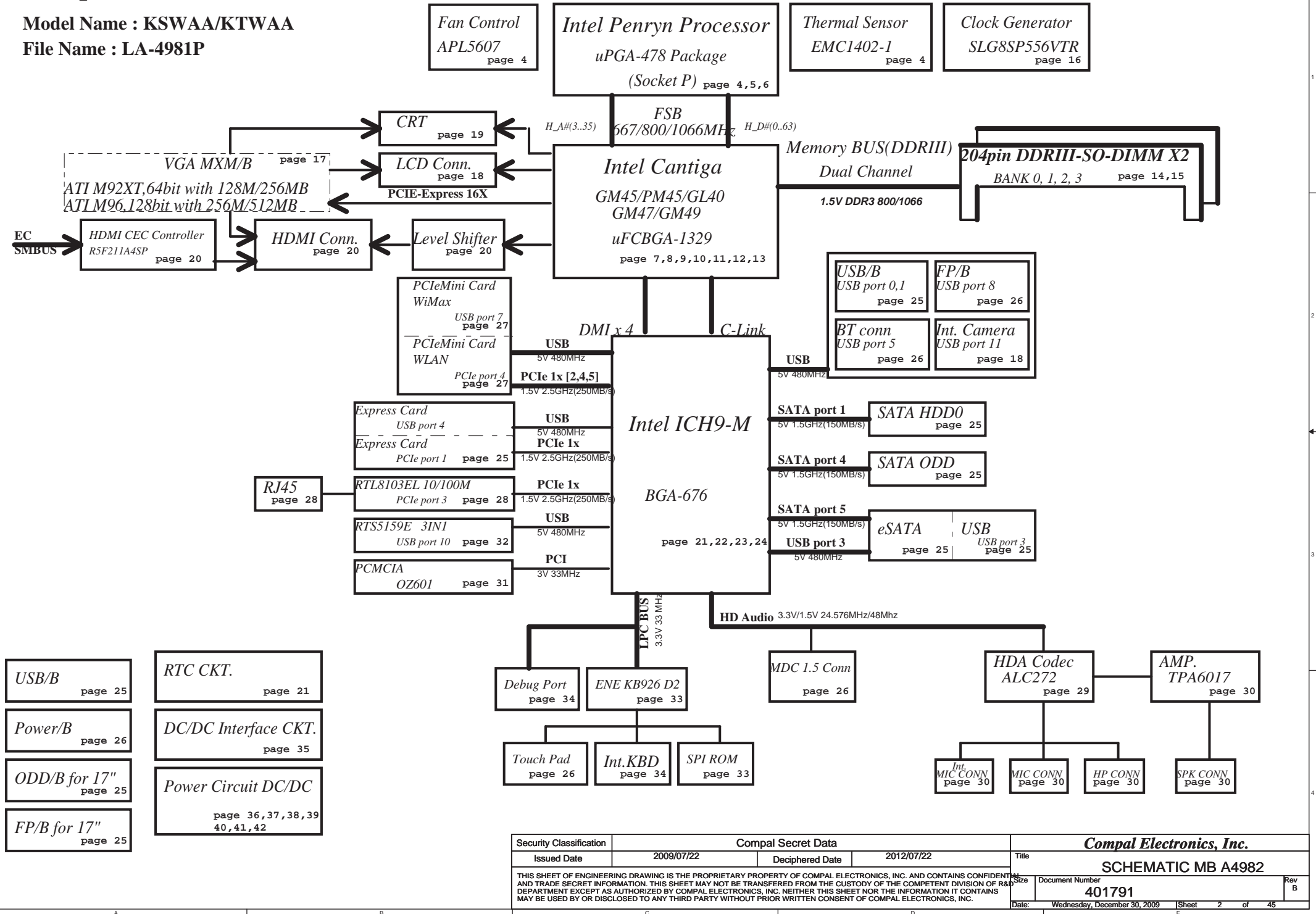
Intel Penryn/ Cantiga/ ICH9M

2009-07-27 Rev. 1.0

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Compal Confidential

Model Name : KSWAA/KTWAA
File Name : LA-4981P



Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8V power rail for VRAM	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+3VS_HDP	3.3V power rail for G-sensor	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VL	5V always on power rail	ON	ON	ON	ON
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

BTO Option Table

Function	Express Card/ PCMCIA		Bluetooth	RJ11	Camera	3D Sensor
description	(E)	(A)	(B)	(R)	(X)	(S)
explain	Express Card	PCMCIA	Bluetooth	MDC	Camera	3D Sensor
BTO	NEW@	PCM@	BT@	MDC@	CAM@	GSSENSOR@

Function	HDMI				
description	(Y)				
explain	Intel(UMA)	ATI VGA/B		COMMON	
BTO	IHDMI@	NIHDMI@	HDMI@	H@	

External PCI Devices

DEVICE	PCI DEVICE ID	IDSEL#	REQ/GNT#	PIRQ
CARD BUS	D4	AD20	1	A/B

EC SM Bus1 address

EC SM Bus2 address

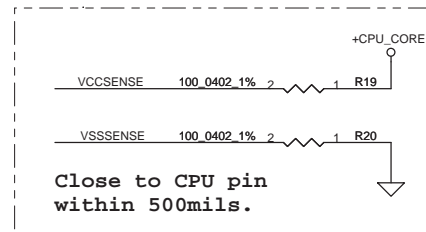
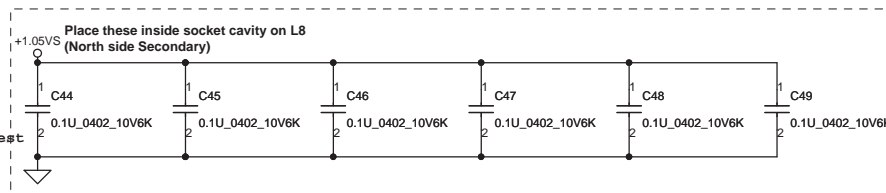
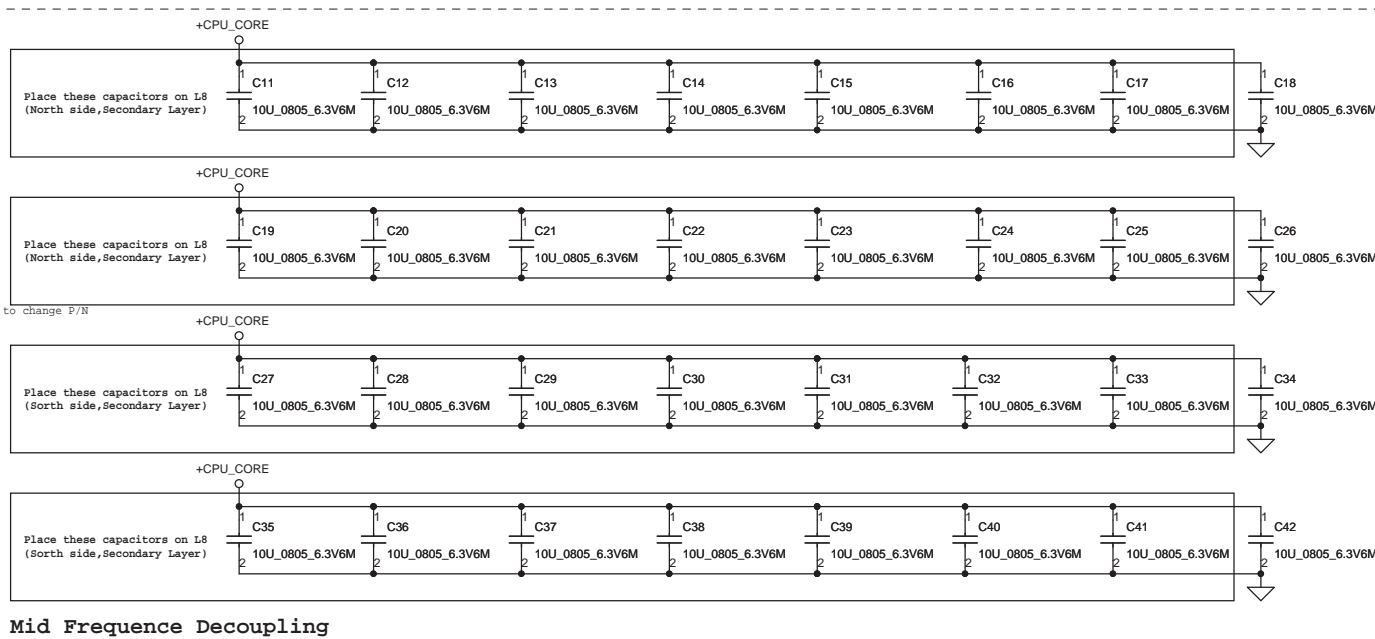
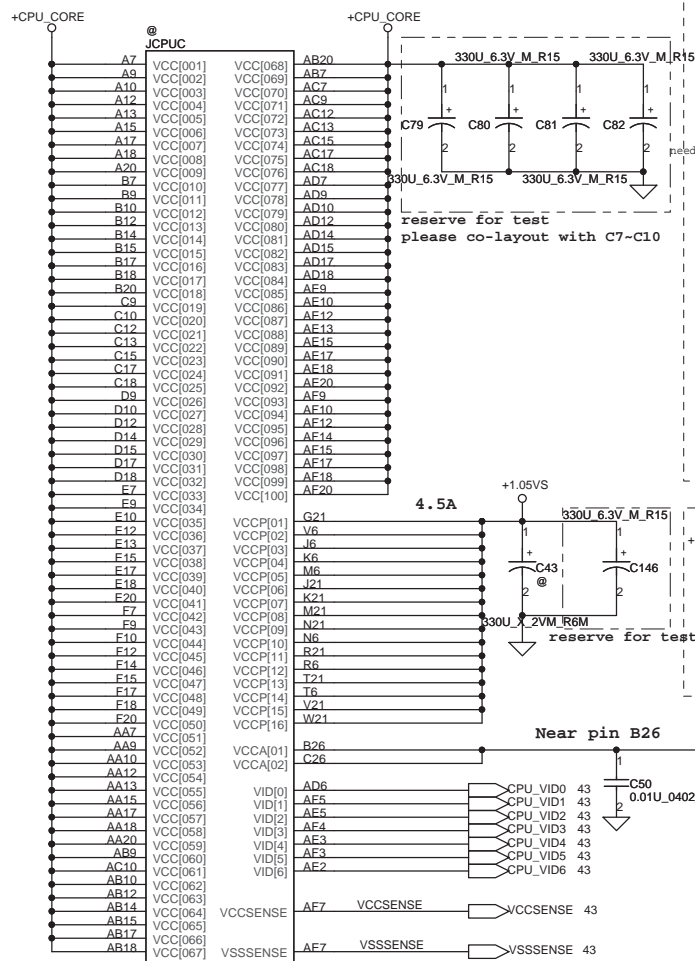
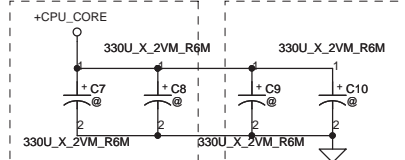
Power	Device	Address	Power	Device	Address
+5VL	EC KB926 D2		+3VS	EC KB926 D2	
+5VL	Smart Battery	0001 011X b	+3VS	CPU THM Sen	1001 101Xb
+5VL	HDMI-CEC	0011 010x b	+3VS	SMSC SMC1402	1001 100Xb
			+3VS	VGA THM Sen	
				ADM1032ARMZ	
				VGA on die	1001 111Xb
				thermal sensor	(No used)

ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
+3VS	Clock Generator (SLG8SP556V)	1101 001Xb
+3VS	DDR DIMM0	1001 000Xb
+3VS	DDR DIMM1	1001 010Xb
+3VS	Express Card	

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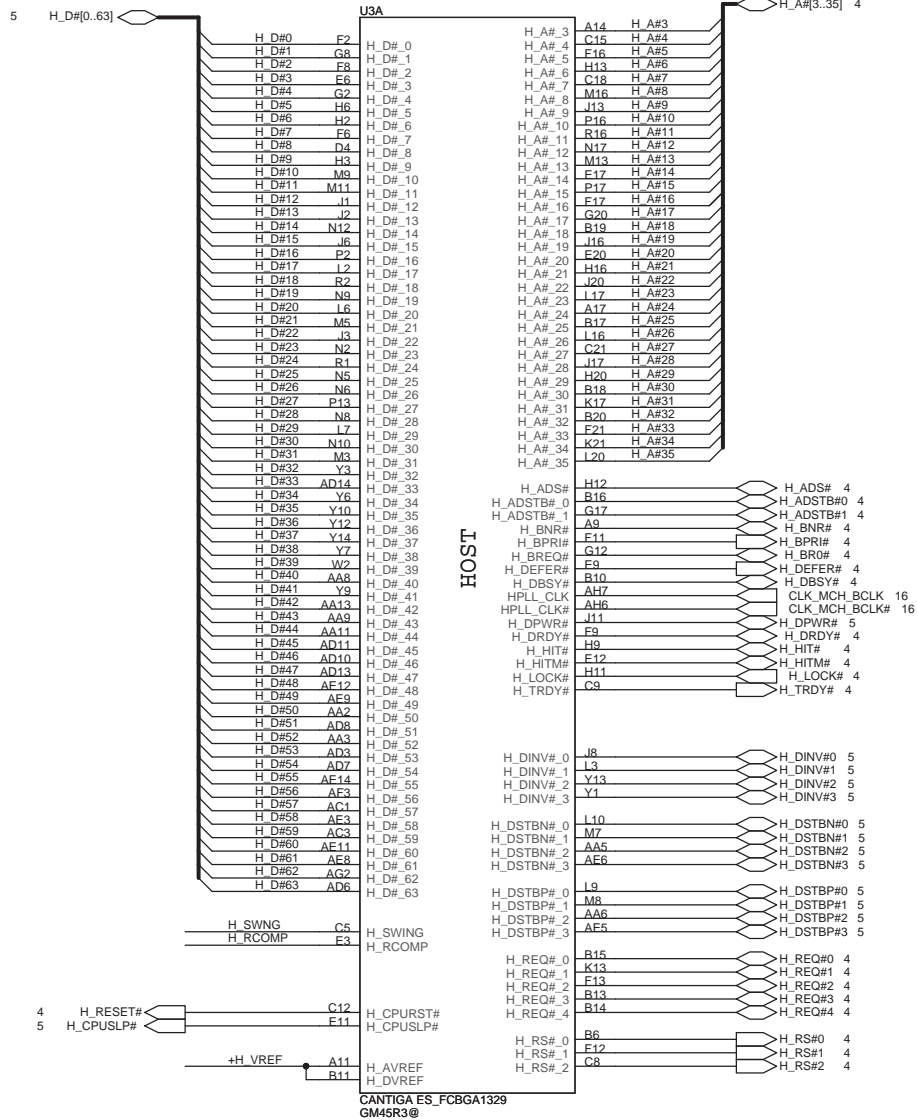
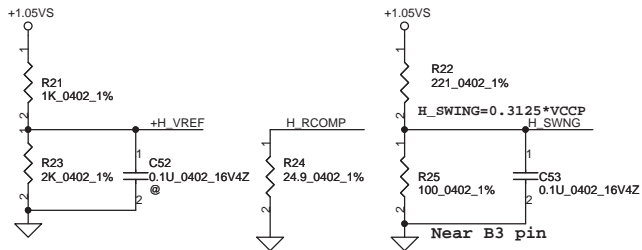
ESR <= 1.5m ohm
Capacitor > 1980uF



Length match within 25 mils.
The trace width/space/other is
14/7/25.

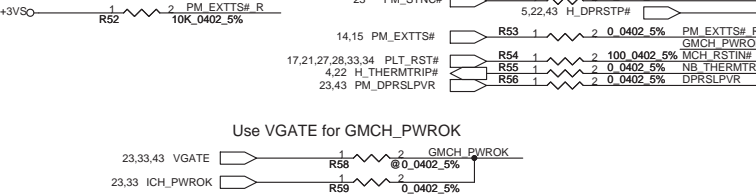
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Layout Note:
H_RCOMP / +H_VREF / H_SWNG
trace width and spacing is 10/20
within 100 mils from NB

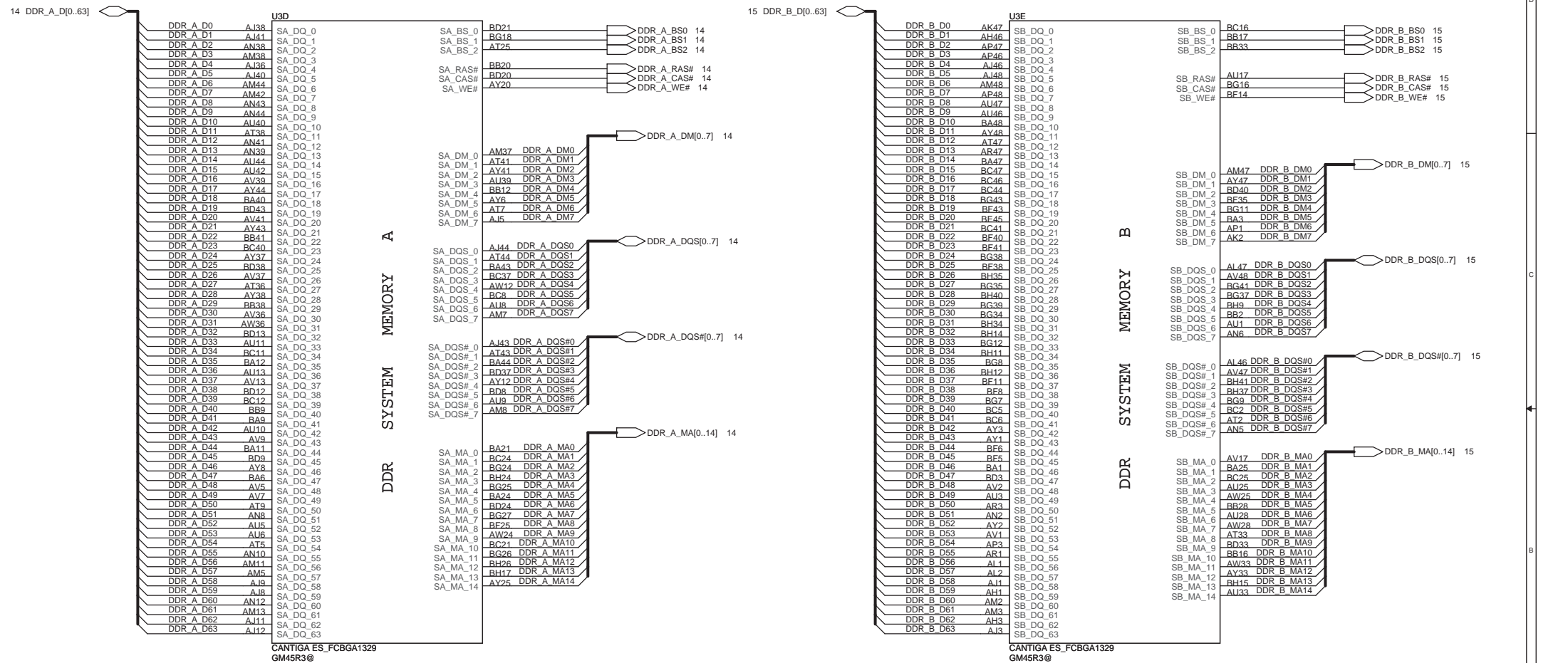


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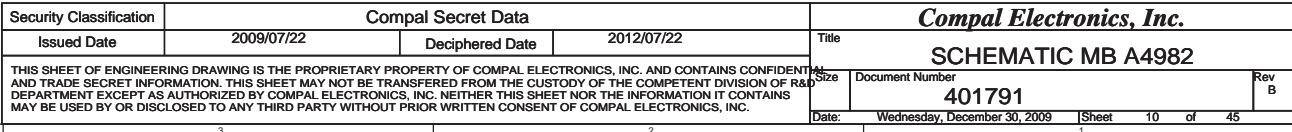
CFG[2:0]		011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6	Internal pull-up	0 = iTPM Host Interface is Enabled can support disble by SW. 1 = iTPM Host Interface is Disabled *(Default)
CFG7	Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9	Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10	Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12]	Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation*(Default)
CFG16	Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19	Internal pull-down	0 = Normal Operation 1 = DMI Lane Reversal Enable *(Default)
CFG20	Internal pull-down (PCIE/SDVO select)	0 = Only PCIE or [SDVO/DP/HDMI] is operational. * (Default) 1 = PCIE/[SDVO/DP/HDMI] are operating simu.

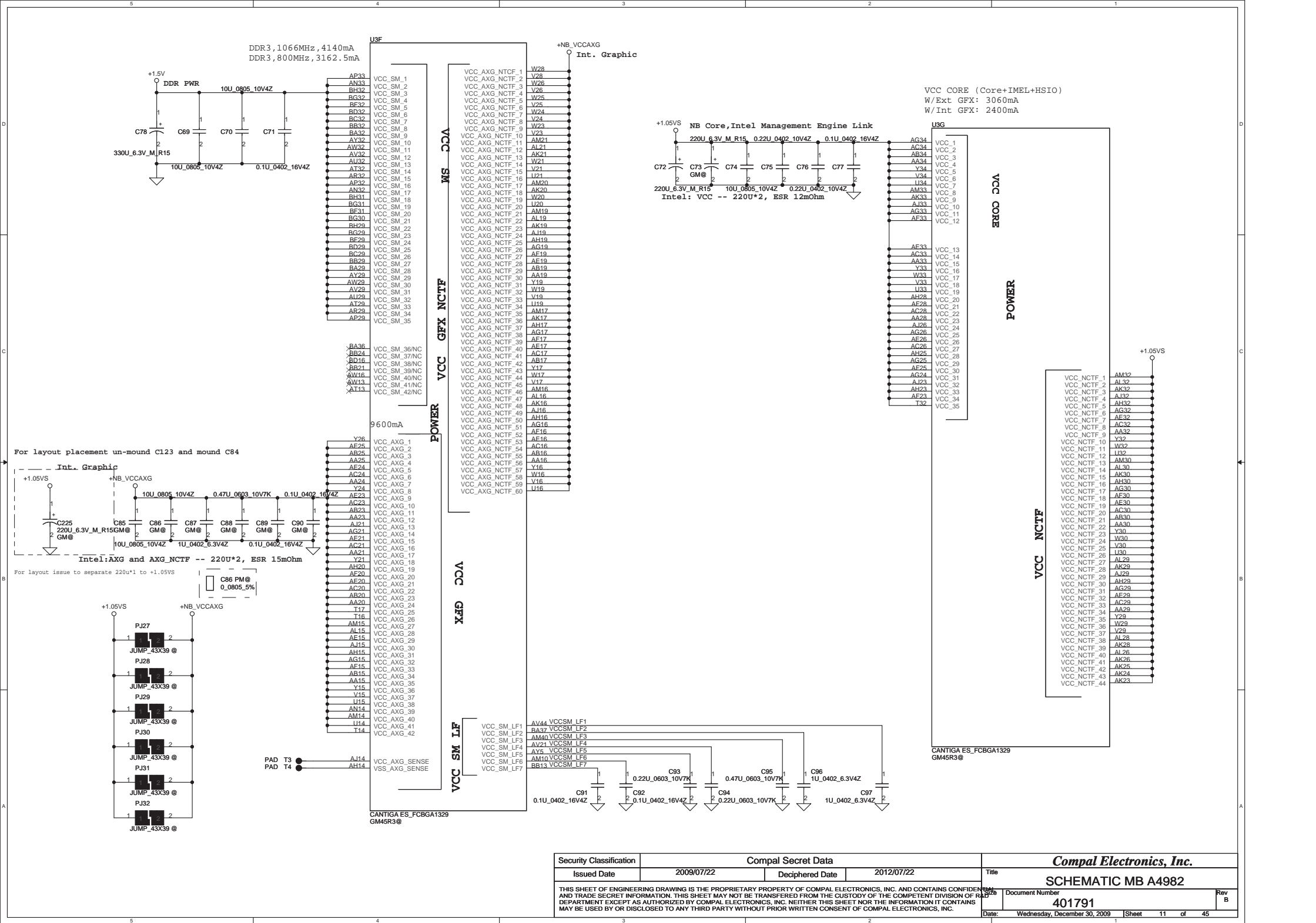


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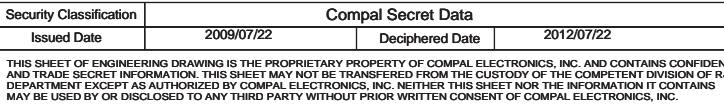


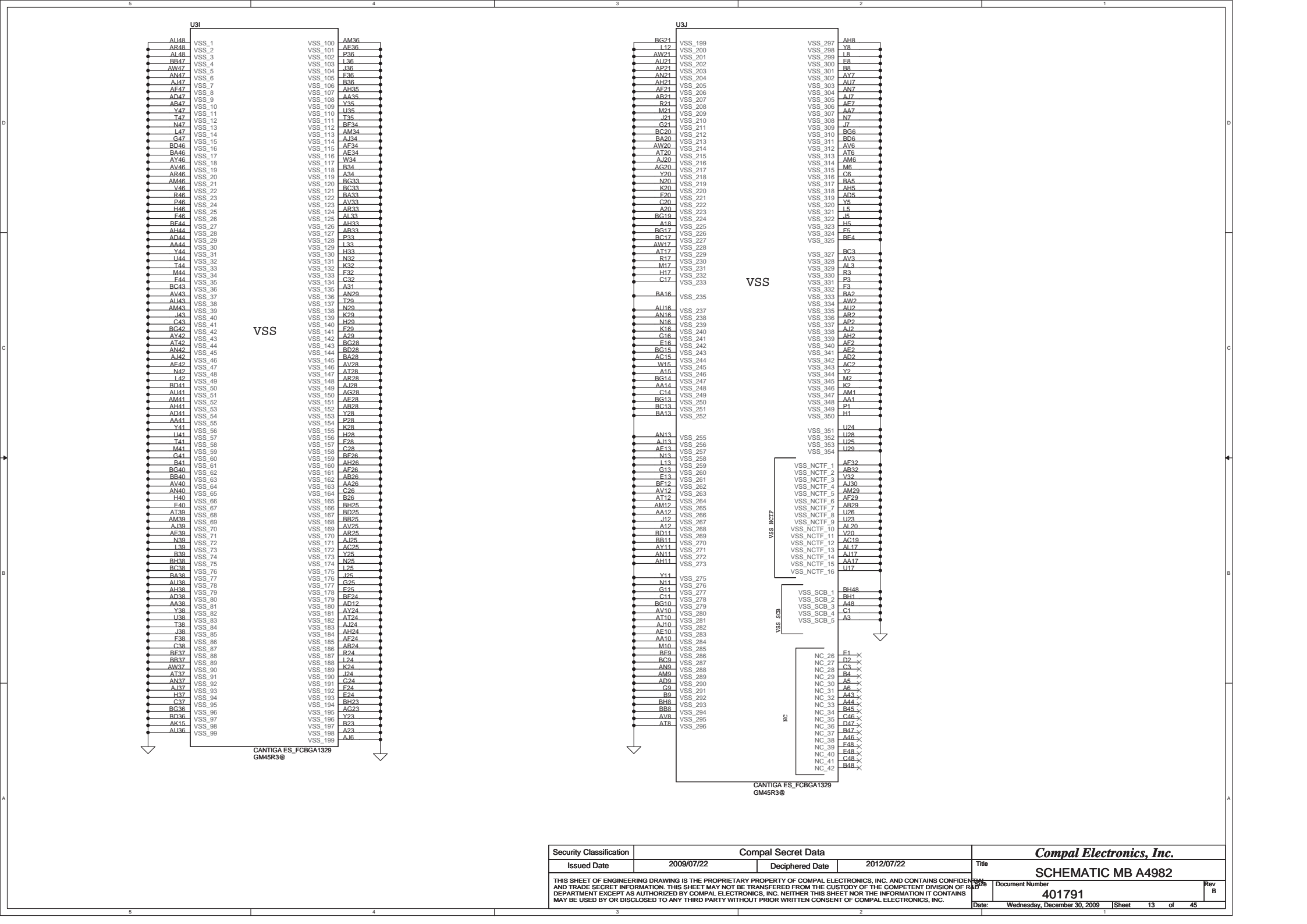
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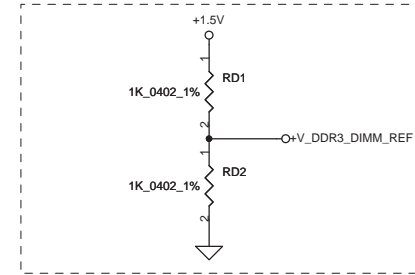
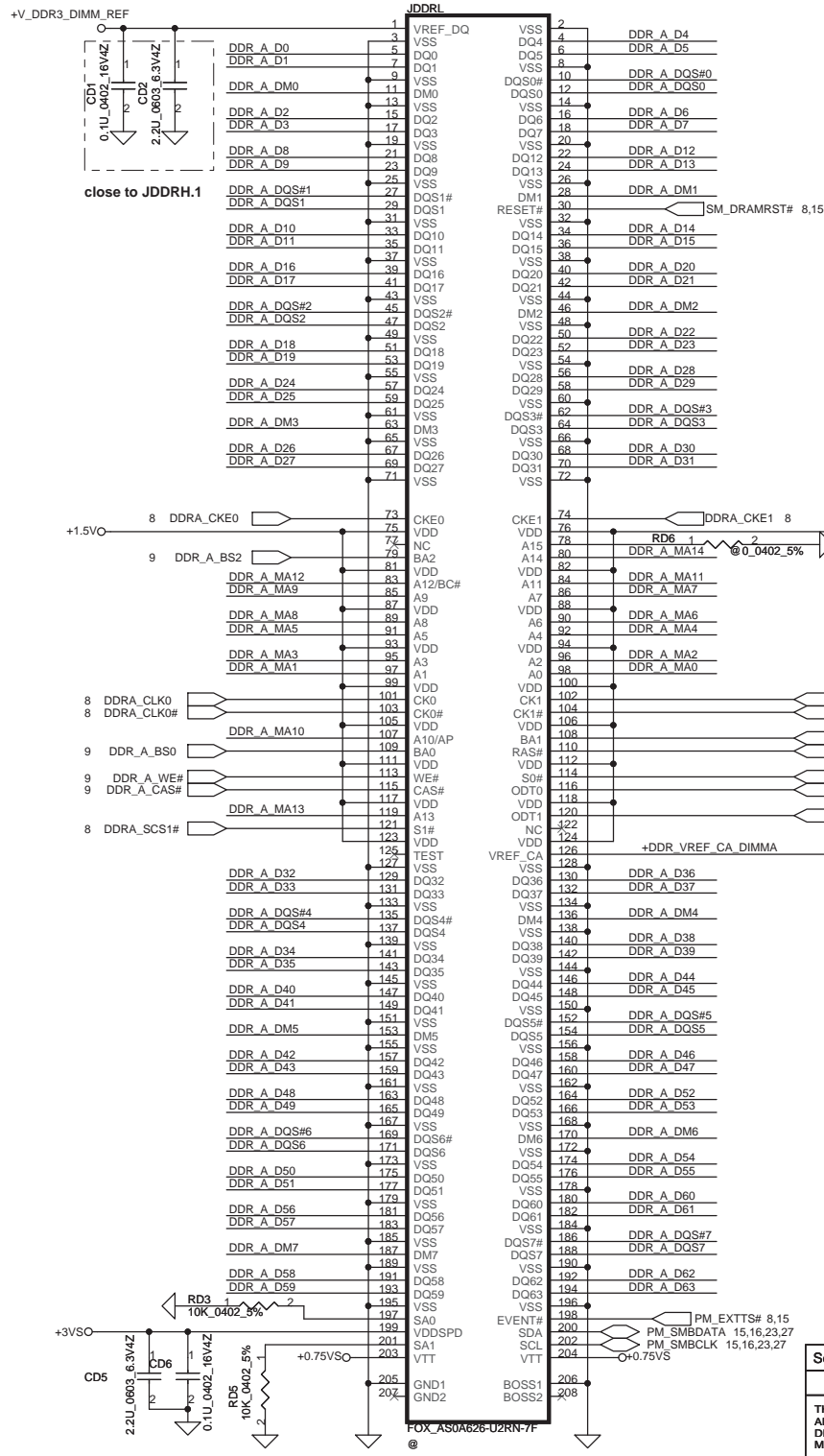


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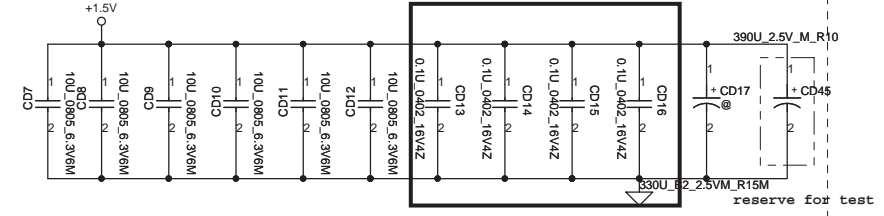


DDR3 SO-DIMM A REVERSE TYPE

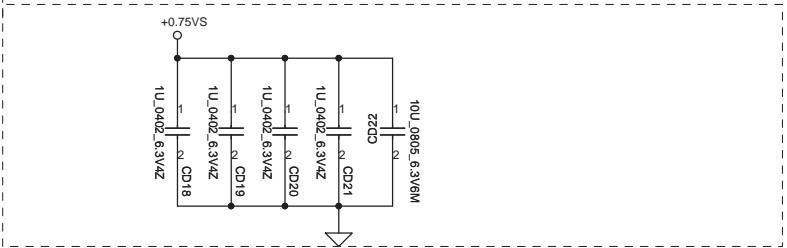


Layout Note:
Place near JDDR1

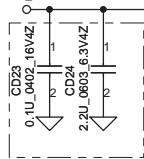
Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA



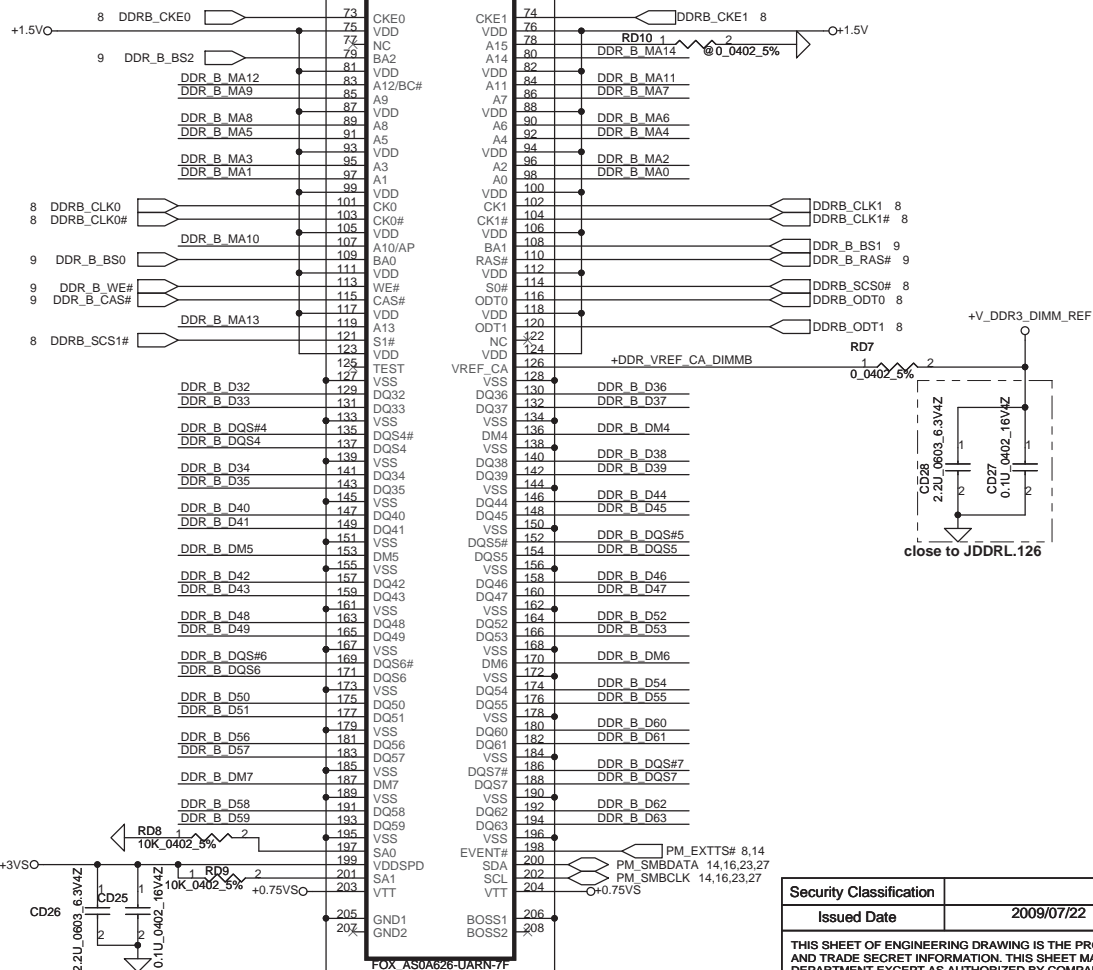
Layout Note:
Place near JDDR1.203 & JDDR1.204



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close to JDDRL.1

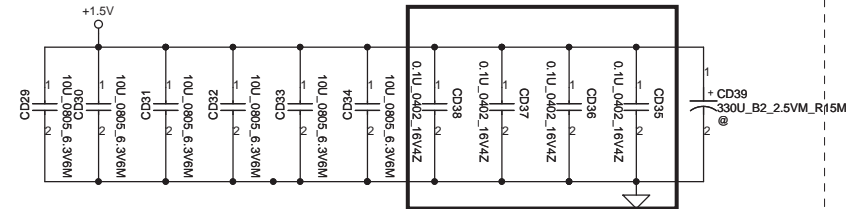


DDR3 SO-DIMM B REVERSE TYPE

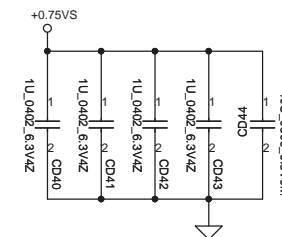


Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB



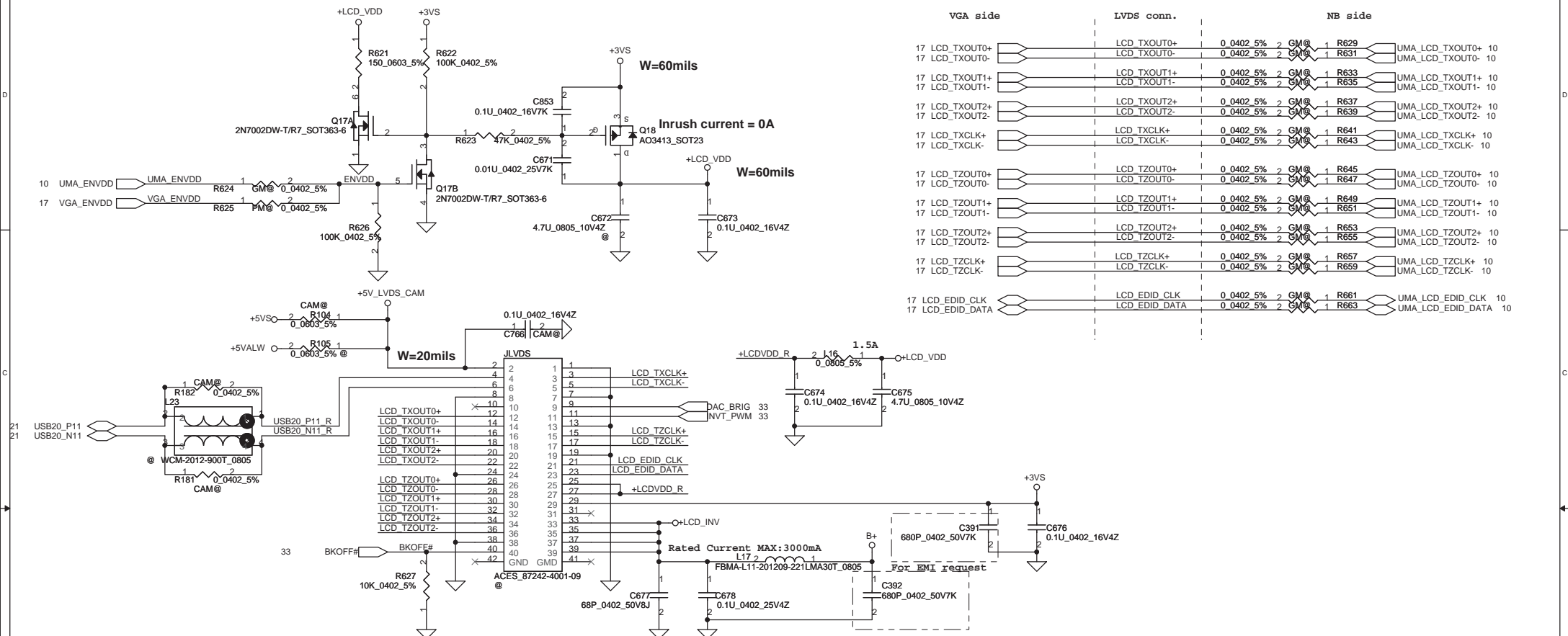
Layout Note:
Place near JDDRH.203 & JDDRH.204












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LCD/PANEL BD. Conn.

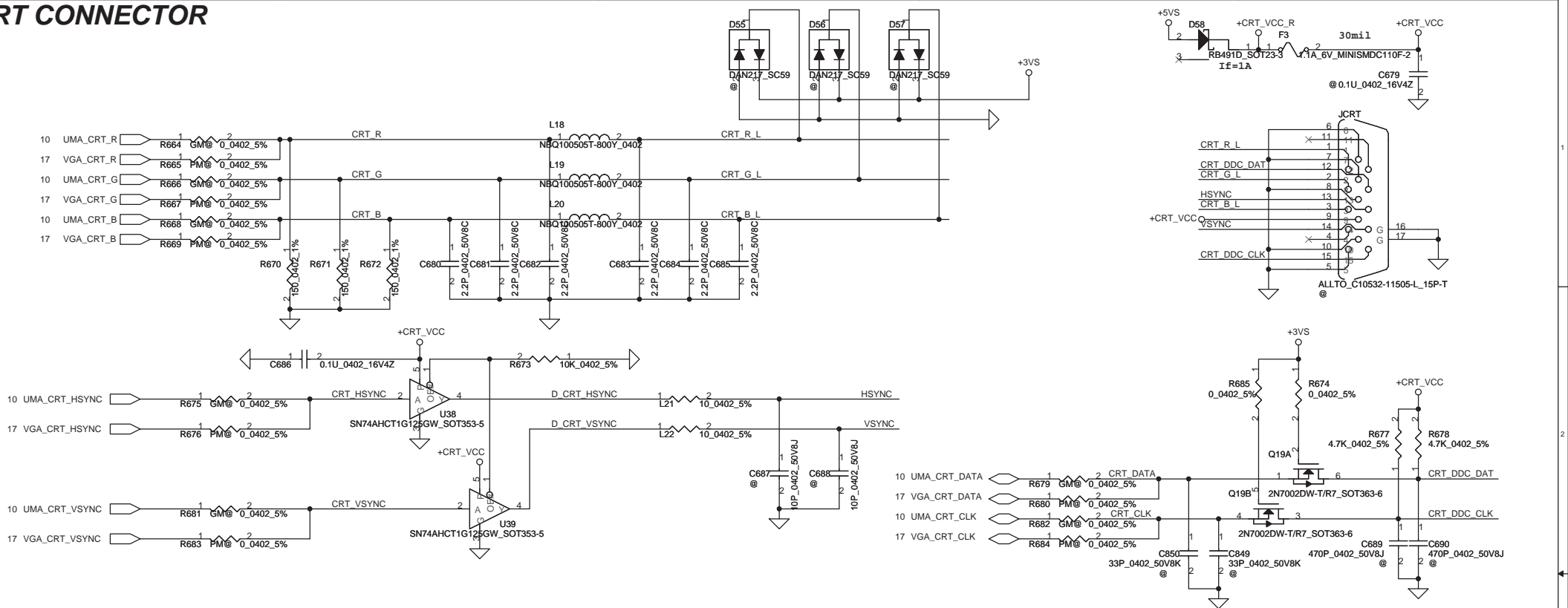
please link to VGA Conn. then link to LVDS Conn.



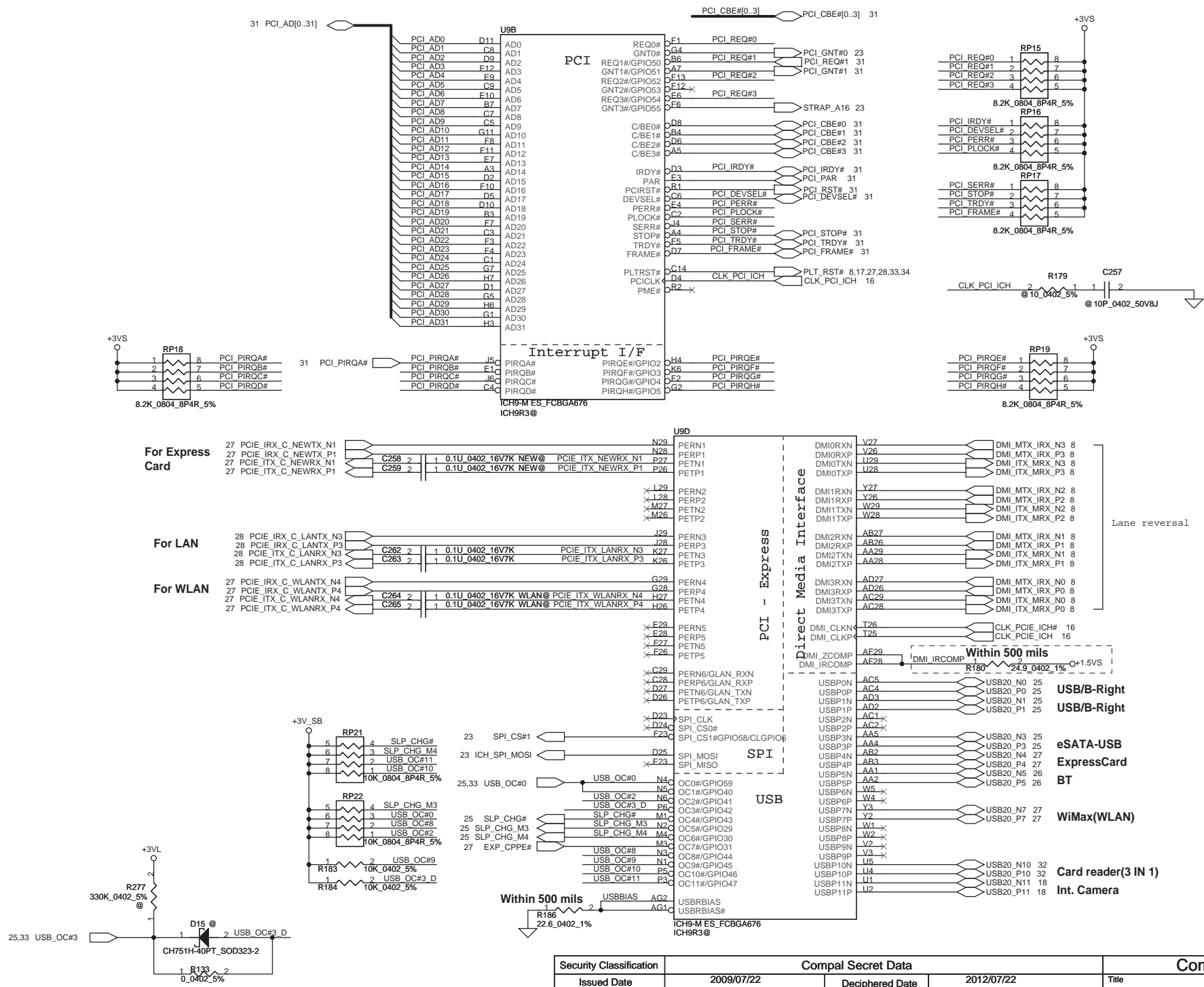
VGA side		LVDS conn.			NB side		
17 LCD_TXOUT0+		LCD TXOUT0+	0.0402 5% 2	GM@	1 R629	UMA_LCD_TXOUT0+	10
17 LCD_TXOUT0-		LCD TXOUT0-	0.0402 5% 2	GM@	1 R631	UMA_LCD_TXOUT0-	10
17 LCD_TXOUT1+		LCD TXOUT1+	0.0402 5% 2	GM@	1 R633	UMA_LCD_TXOUT1+	10
17 LCD_TXOUT1-		LCD TXOUT1-	0.0402 5% 2	GM@	1 R635	UMA_LCD_TXOUT1-	10
17 LCD_TXOUT2+		LCD TXOUT2+	0.0402 5% 2	GM@	1 R637	UMA_LCD_TXOUT2+	10
17 LCD_TXOUT2-		LCD TXOUT2-	0.0402 5% 2	GM@	1 R639	UMA_LCD_TXOUT2-	10
17 LCD_TXCLK+		LCD TXCLK+	0.0402 5% 2	GM@	1 R641	UMA_LCD_TXCLK+	10
17 LCD_TXCLK-		LCD TXCLK-	0.0402 5% 2	GM@	1 R643	UMA_LCD_TXCLK-	10
<hr/>							
17 LCD_TZOUT0+		LCD TZOUT0+	0.0402 5% 2	GM@	1 R645	UMA_LCD_TZOUT0+	10
17 LCD_TZOUT0-		LCD TZOUT0-	0.0402 5% 2	GM@	1 R647	UMA_LCD_TZOUT0-	10
17 LCD_TZOUT1+		LCD TZOUT1+	0.0402 5% 2	GM@	1 R649	UMA_LCD_TZOUT1+	10
17 LCD_TZOUT1-		LCD TZOUT1-	0.0402 5% 2	GM@	1 R651	UMA_LCD_TZOUT1-	10
17 LCD_TZOUT2+		LCD TZOUT2+	0.0402 5% 2	GM@	1 R653	UMA_LCD_TZOUT2+	10
17 LCD_TZOUT2-		LCD TZOUT2-	0.0402 5% 2	GM@	1 R655	UMA_LCD_TZOUT2-	10
17 LCD_TZCLK+		LCD TZCLK+	0.0402 5% 2	GM@	1 R657	UMA_LCD_TZCLK+	10
17 LCD_TZCLK-		LCD TZCLK-	0.0402 5% 2	GM@	1 R659	UMA_LCD_TZCLK-	10
<hr/>							
17 LCD_EDID_CLK		LCD EDID_CLK	0.0402 5% 2	GM@	1 R661	UMA_LCD_EDID_CLK	10
17 LCD_EDID_DATA		LCD EDID_DATA	0.0402 5% 2	GM@	1 R663	UMA_LCD_EDID_DATA	10

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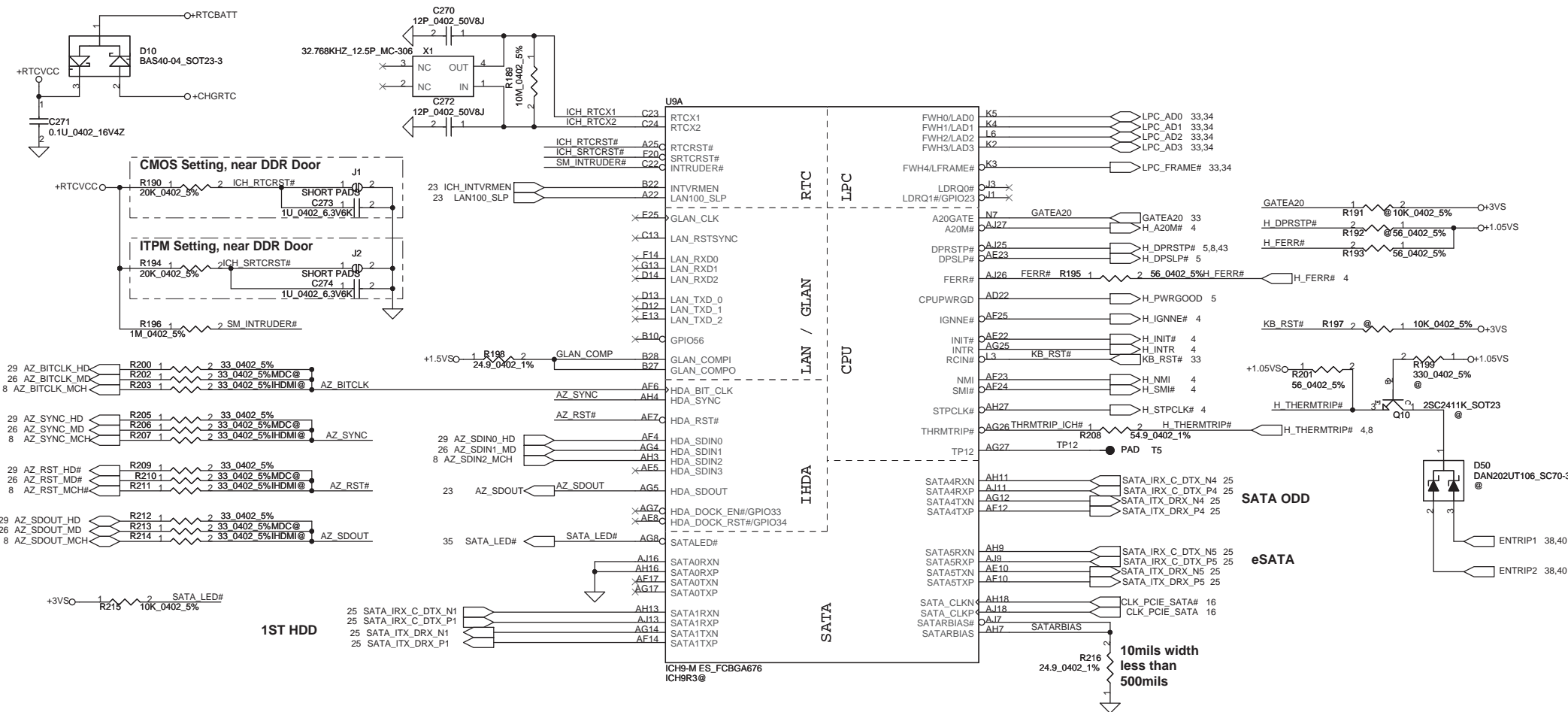
CRT CONNECTOR



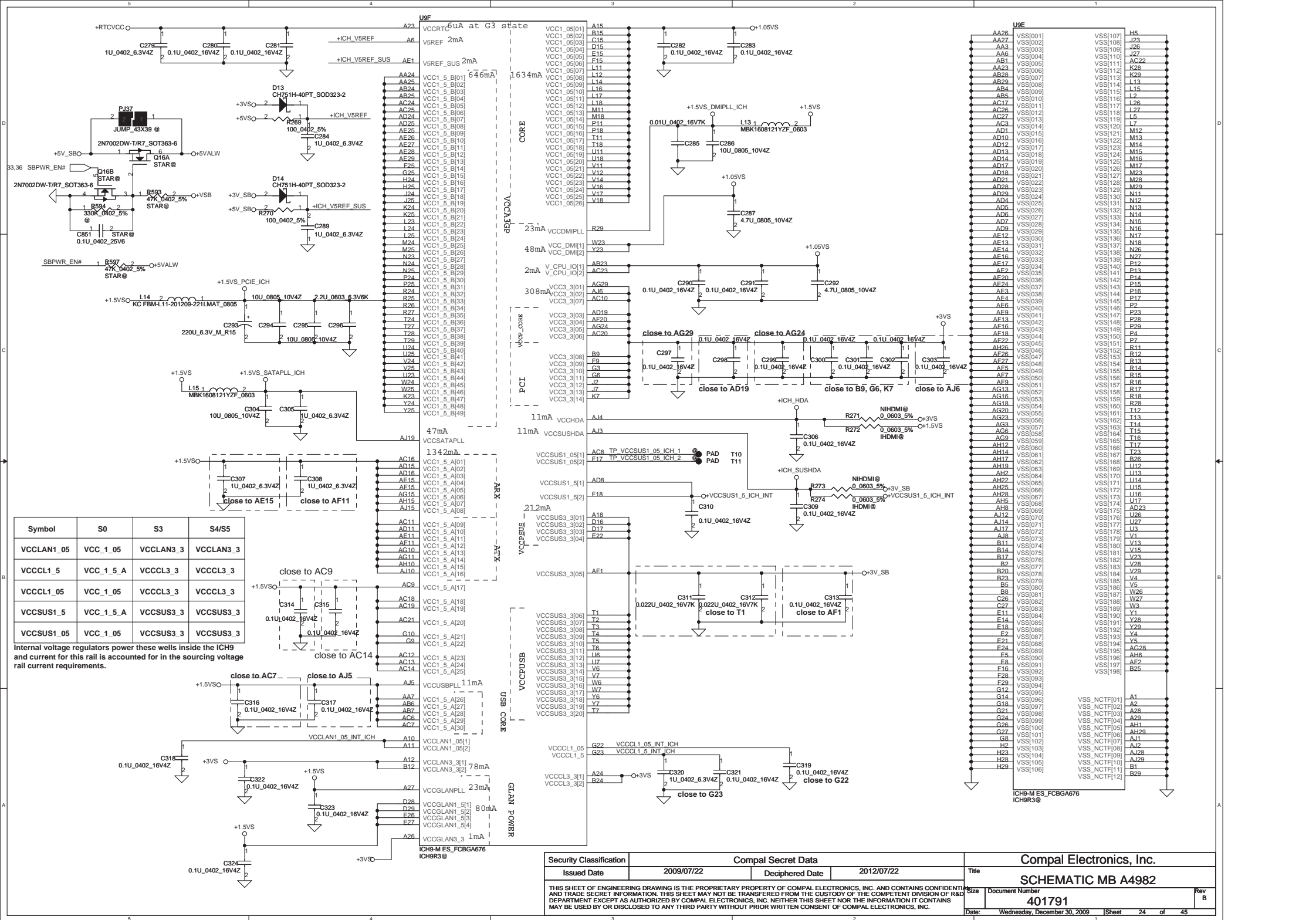
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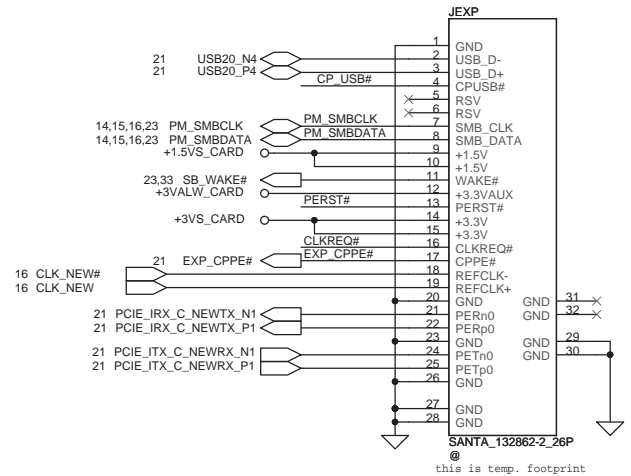
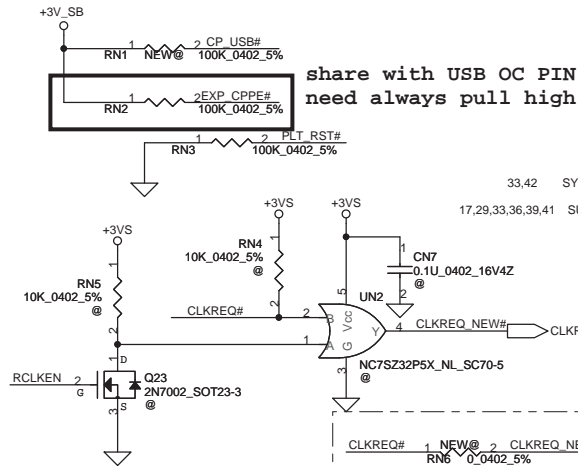
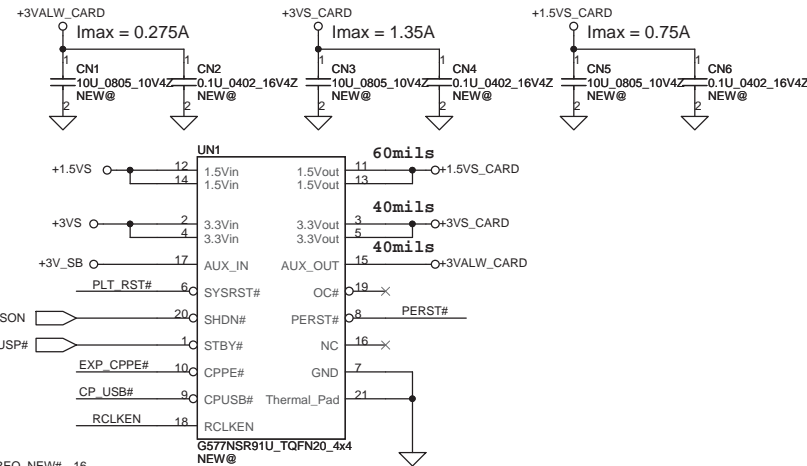
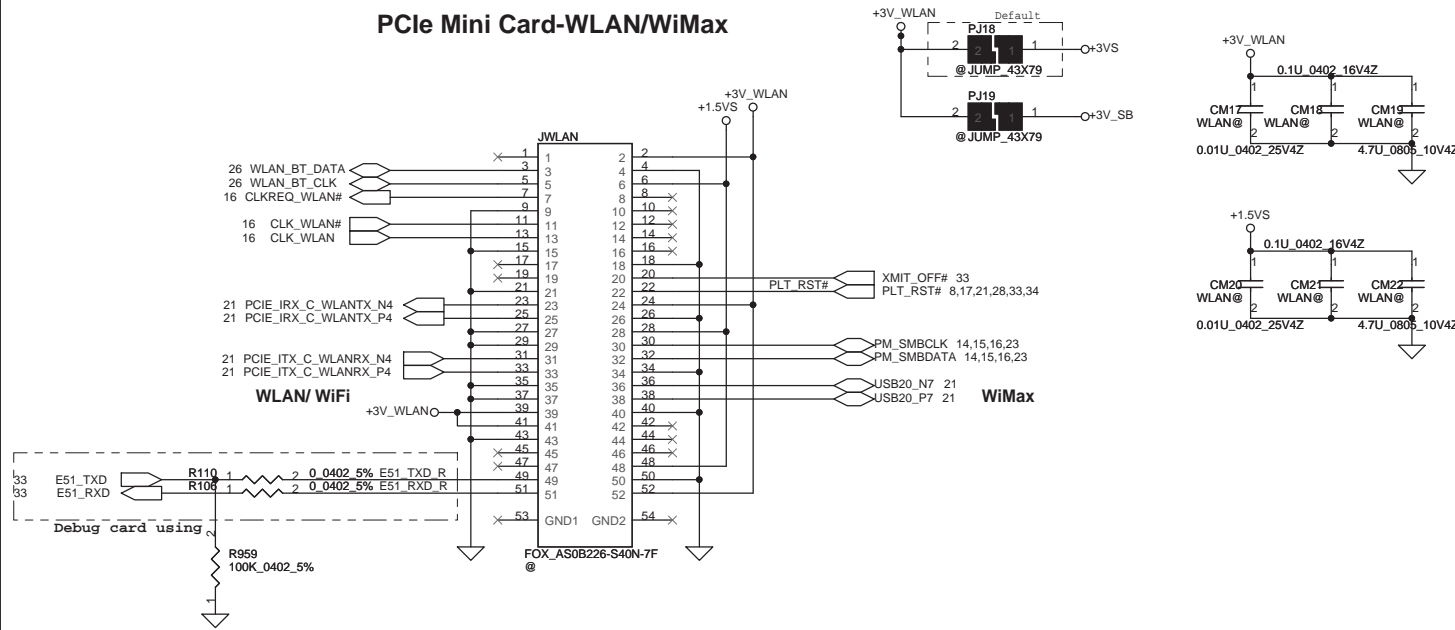
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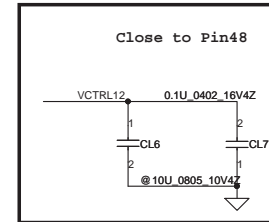
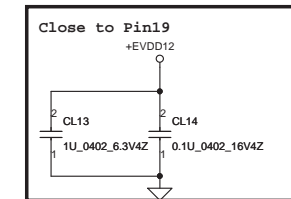
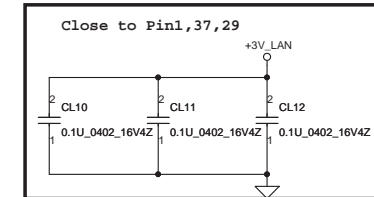
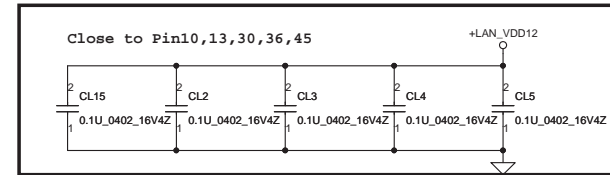
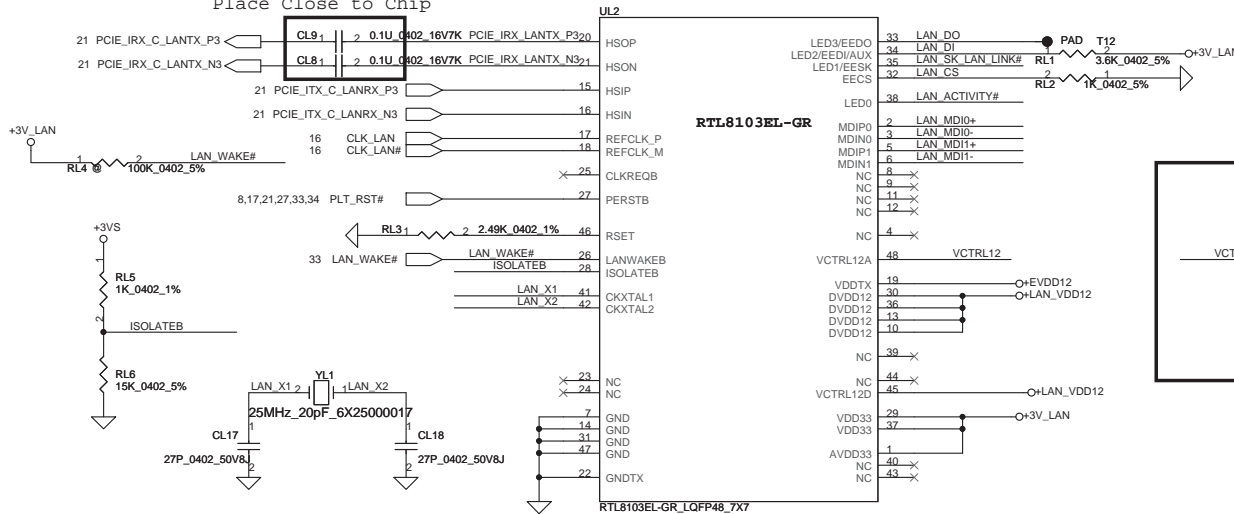


PCle Mini Card-WLAN/WiMax

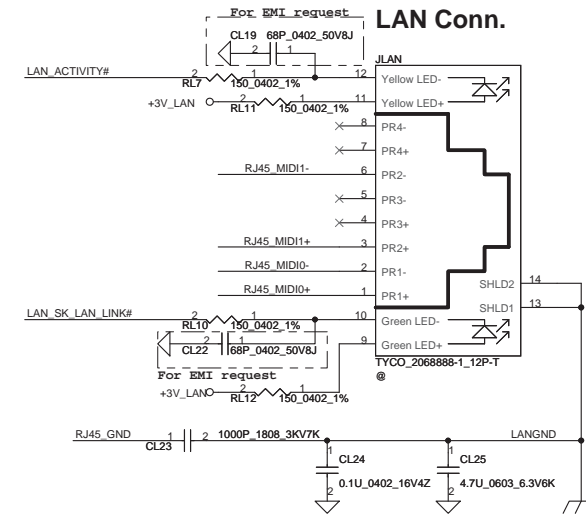
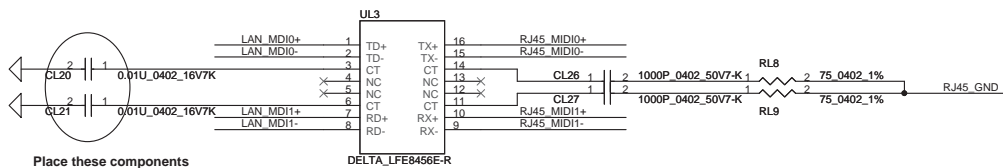


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Place Close to Chip

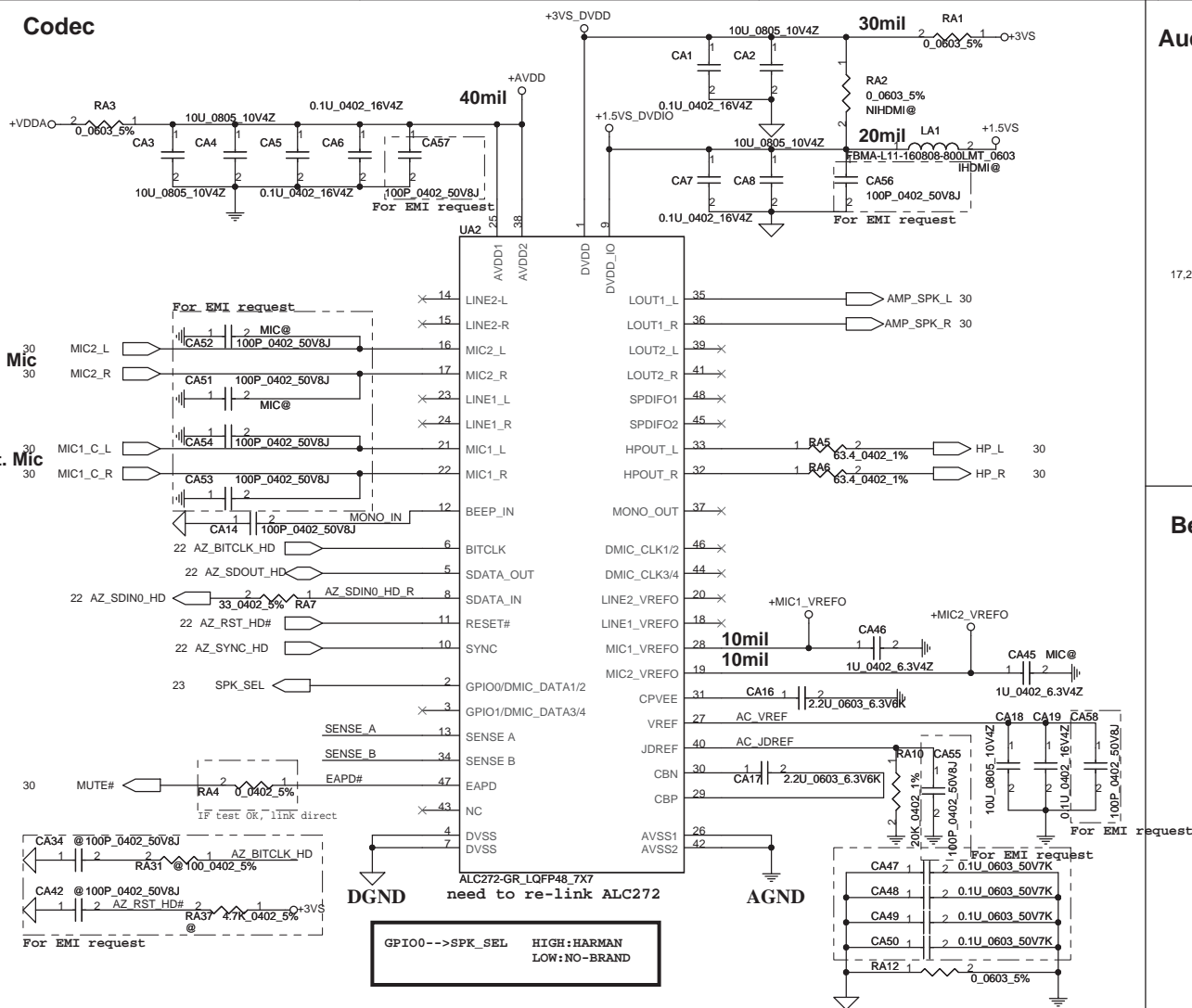


Place these components
close to UL3

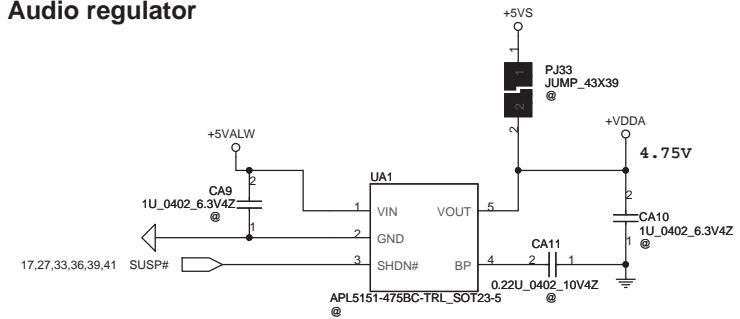


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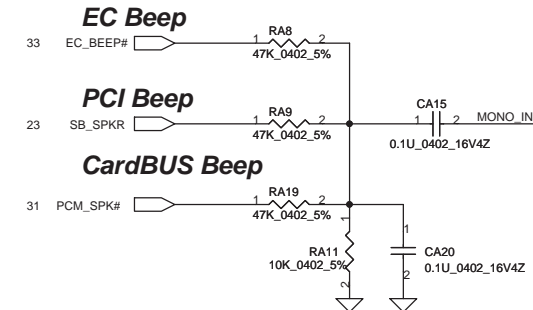
Codec



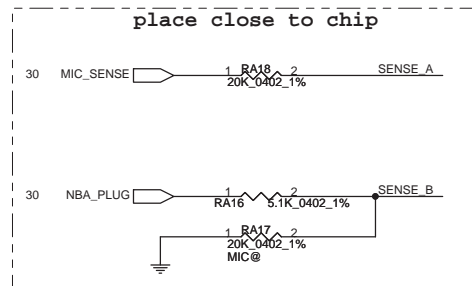
Audio regulator



Beep sound



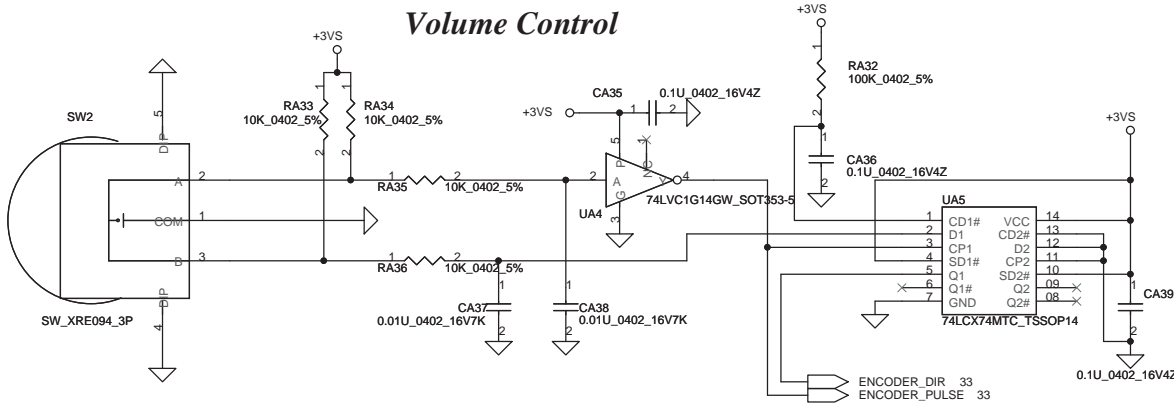
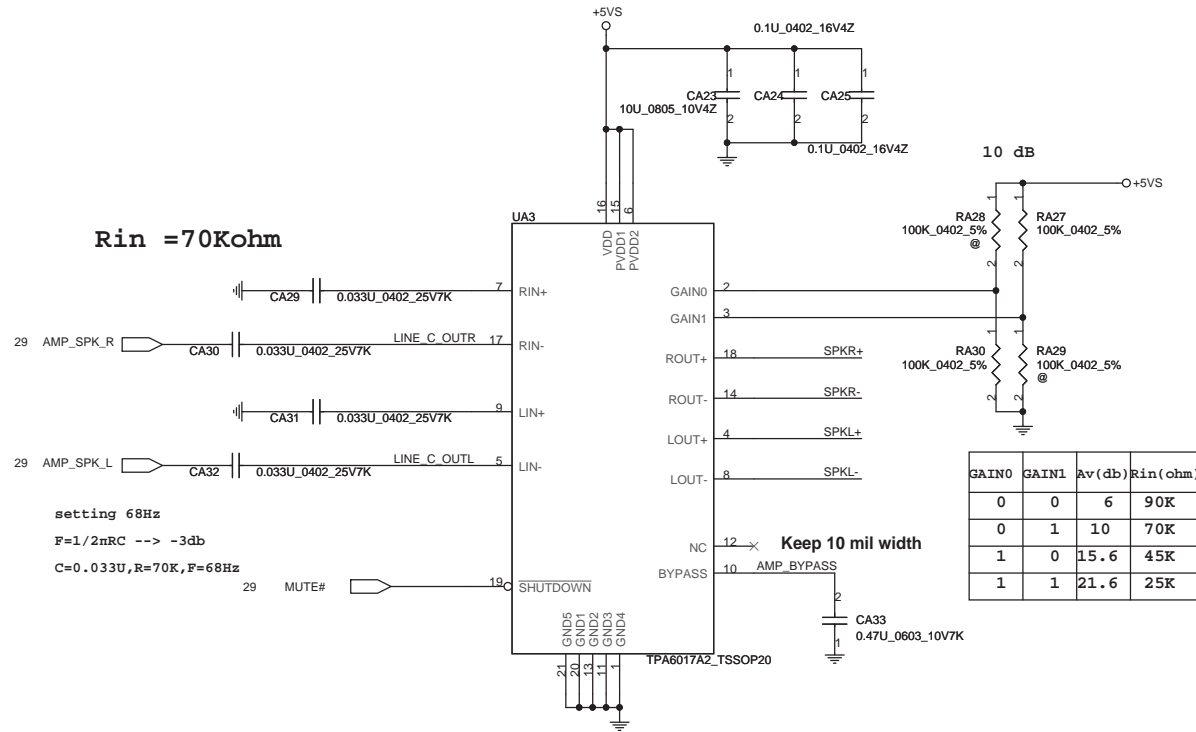
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
SENSE B	5.1K	PORT-D (PIN 35, 36)	SPK out
	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out



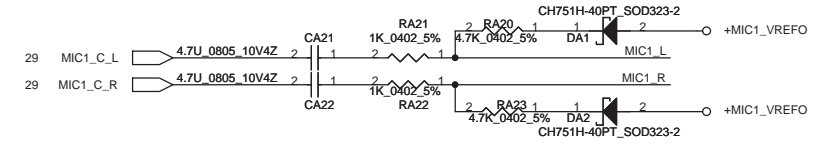
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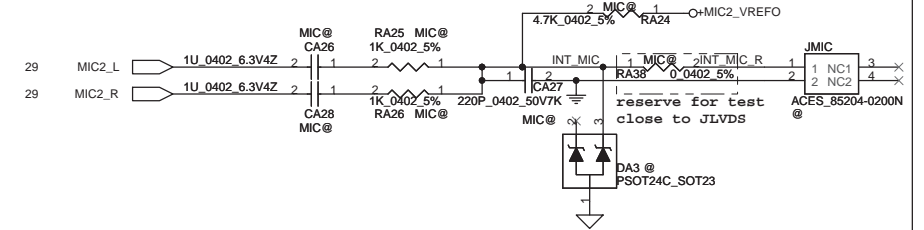
TPA6017 Medium Range Amplifier



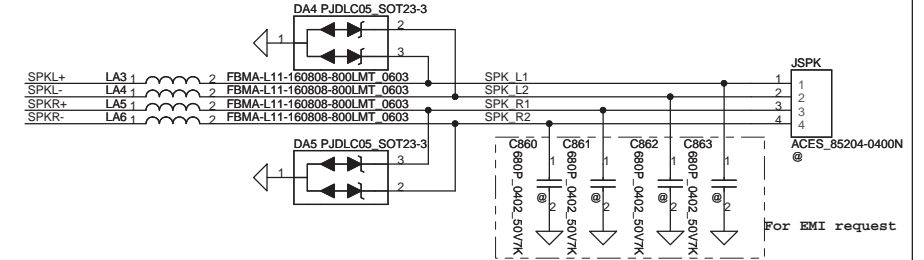
Ext. Mic



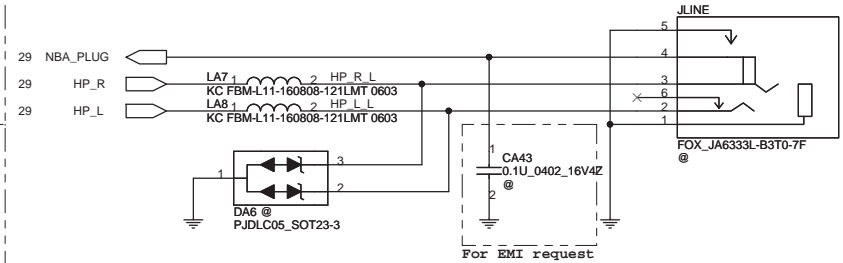
Int. Mic



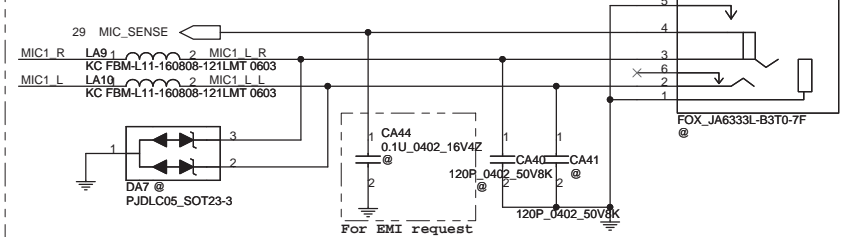
Speaker Connector



HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK

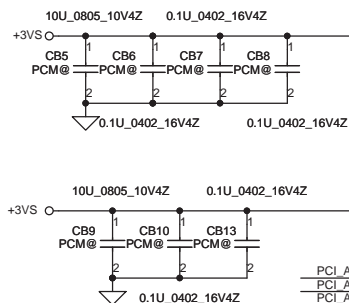


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21 PCI_AD[0..31] PCI_AD[0..31]

21 PCI_CBE#[0..3] PCI_CBE#[0..3]

IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)



UB1

CORE_VCC
CORE_VCC
CORE_VCC
CORE_VCC

VCC5#/VCCD0#/SDATA
VCC3#/VCCD1#/SCLK
VPP_PGM/VPPD0/SLATCH

D10/CAD31
D9/CAD30
D1/CAD29
D8/CAD28
D0/CAD27
A0/CAD26
A1/CAD25
A2/CAD24
A3/CAD23
A4/CAD22
A5/CAD21
A6/CAD20
A7/CAD19
A8/CAD18
A9/CAD17
A10/CAD16
A11/CAD15
A12/CAD14
A13/CAD13
A14/CAD12
A15/CAD11
A16/CAD10
A17/CAD9
A18/CAD8
A19/CAD7
A20/CAD6
A21/CAD5
A22/CAD4
A23/CAD3
A24/CAD2
A25/CAD1
A26/CAD0

PCI_AD20 1 PCM@ 2
RB19 100_0402_5%
IDSEL 127
VPP_VCC/VPPD1/IDSEL
C/BE#3 11
C/BE#2 12
C/BE#1 49
C/BE#0 50

16 CLK_PCI_PCM
21 PCI_DEVSEL#
21 PCI_FRAME#
21 PCI_IRDY#
21 PCI_TRDY#
21 PCI_STOP#
21 PCI_PAR#
29 PCM_SPK#
21 PCI_REQ#1
21 PCI_GNT#1
21 PCI_RST#
23 PM_CLKRUN#
23,33,34 SERIRQ
21 PCI_PIRQA#

107 S1 A16
114 S1 A23
117 S1 A15
116 S1 A22
113 S1 A21
61 S1 A20
58 S1 A19
60 S1 A14
91 S1 WAIT#
89 S1 INPACK#
62 S1 WE#
88 S1 RDY#
59 S1 A19
97 S1 WP
119 S1 RST
98 S1 D2
86 S1 D14
63 S1 A18
57 S1 VS1
121 S1 VS2
56 S1 CD1#
122 S1 CD2#
92 S1 BVD2
90 S1 BVD1
111 S1 REG#
112 S1 A12
66 S1 A8
67 S1 CE1#

BVD1/STSCG#
BVD2/LEDCAUDIO
BVD1/STSCG#

REG#CCBE3#
A12/CCBE2#
A8/CCBE1#
CE1/CCBE0#

OZ6011N_TQFP128-D
PCM@

RB18 33_0402_5%
PCM@ 2 S1 A16

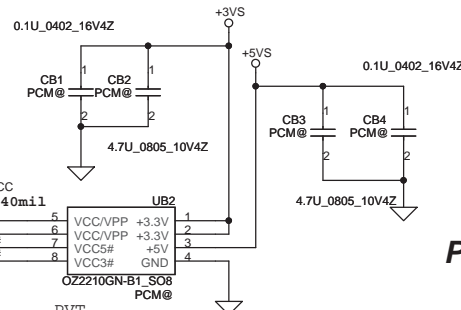
VCC5# (124)	VPP_PGM (125)	IDSEL SELECT
0	0	AD18
0	1	*AD20
1	0	AD25
1	1	PIN F4

NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME.
IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE
PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

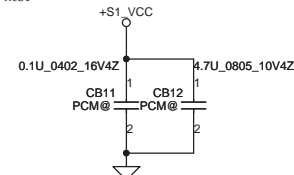
22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE
REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO
SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS.
THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS
FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY
CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST
BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

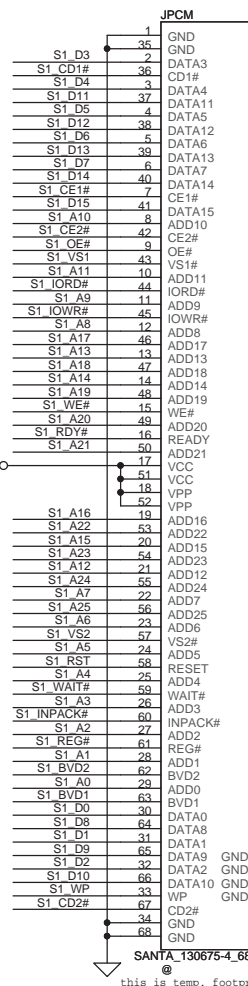


SA000026P10 (S IC OZ2210GN-B1 SO 8P)

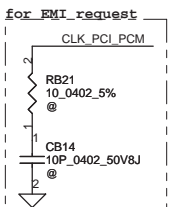
IDSEL SELECT



PCMCIA Socket

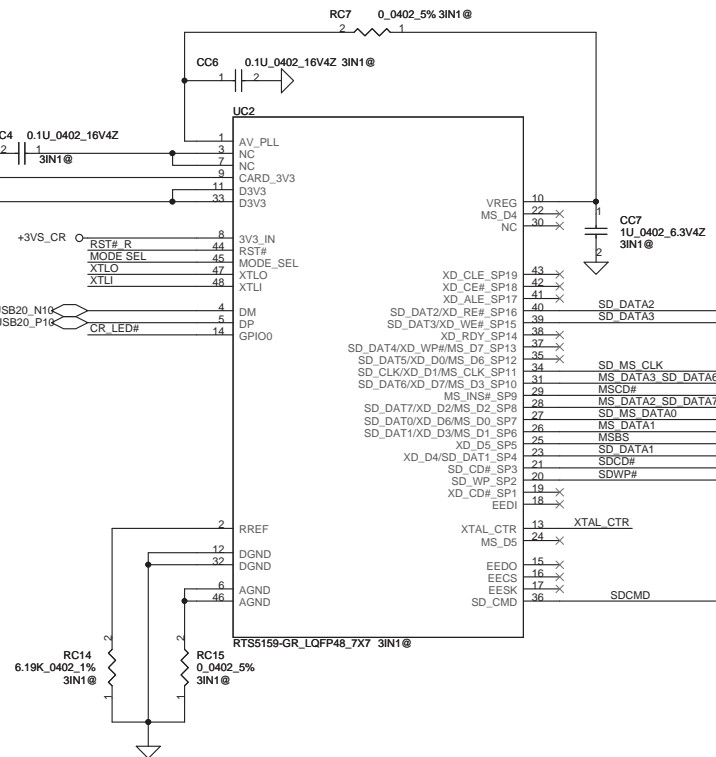
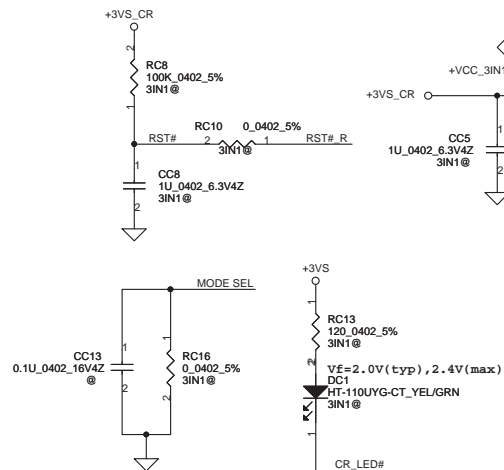
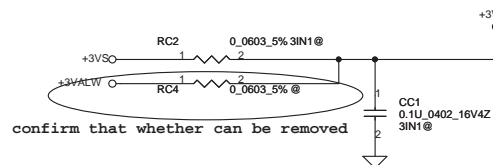


this is temp. footprint



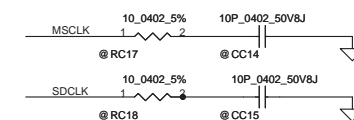
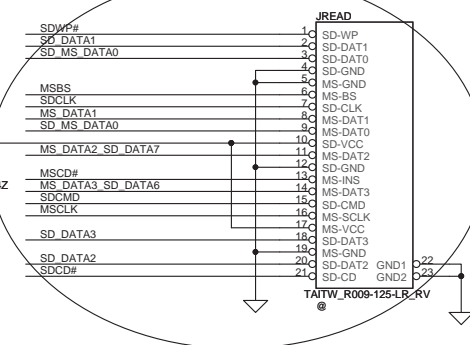
22K TO 47K PULL-UPS MUST BE PLACED
ON INTA#, PME#, SERIRQ# & CLKRUN#.

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				45							

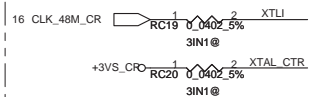


3 in 1 Card Reader

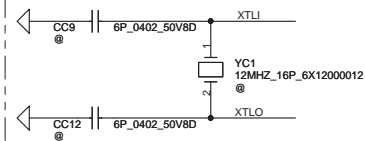
confirm all pin define with connector spec.



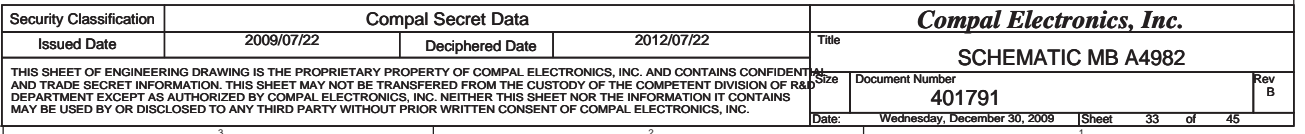
48Mhz



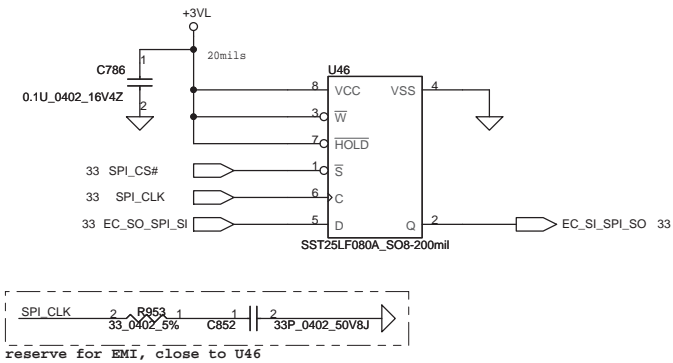
12Mhz



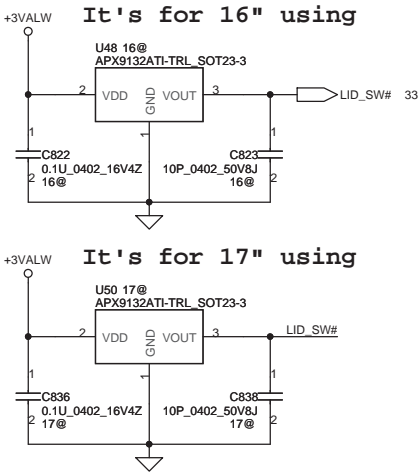
R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	



SPI Flash (16Mb*1)

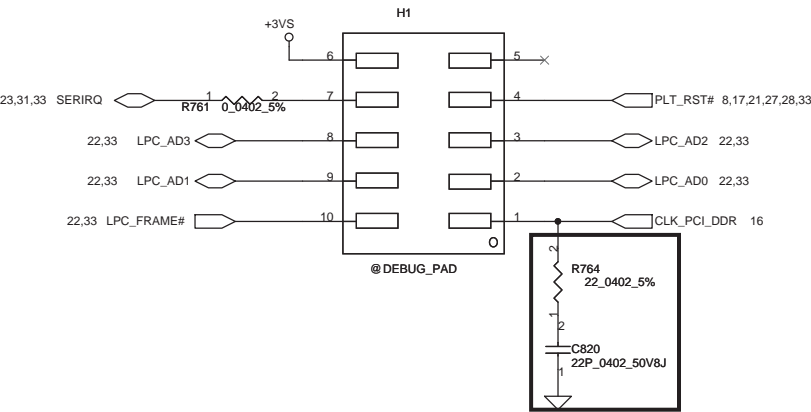


Lid SW



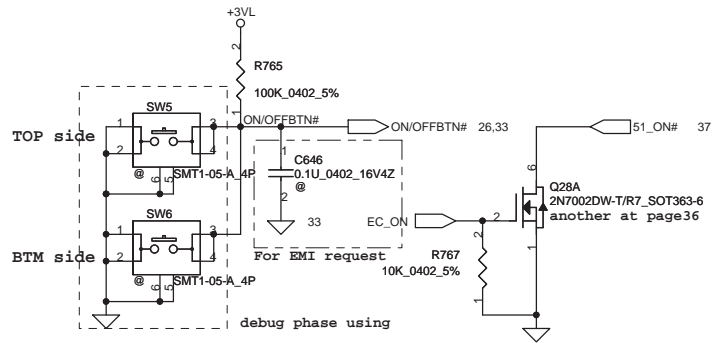
LPC Debug Port

Please place the PAD under DDR DIMM.

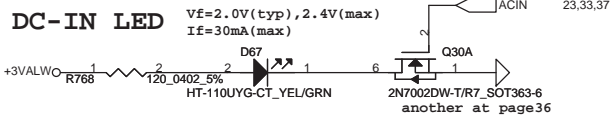
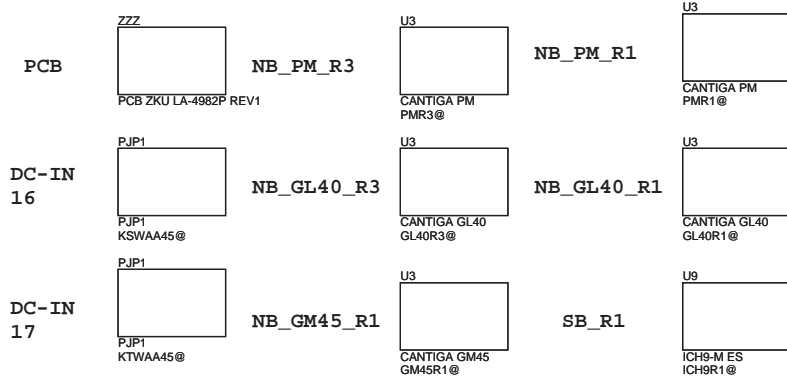


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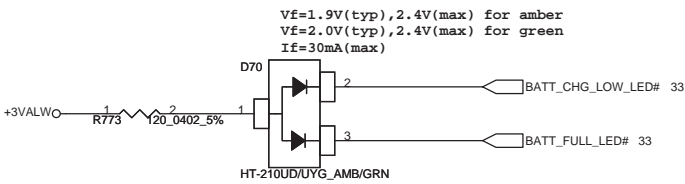
Power Button



ISPD



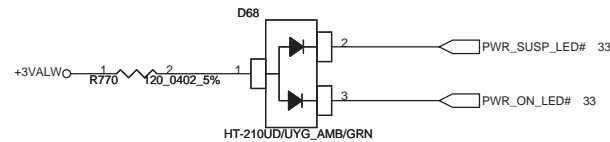
BATT CHARGE/FULL LED



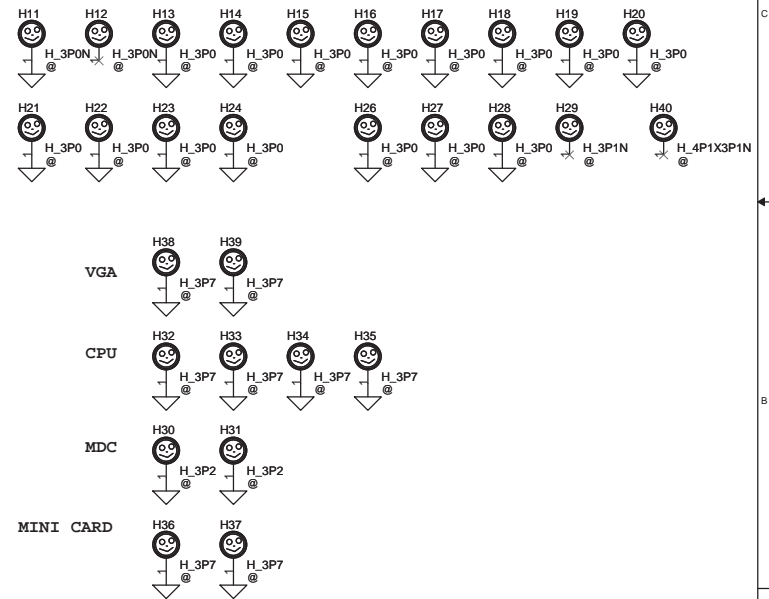
WL&BT LED



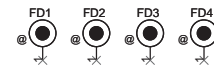
POWER/SUSPEND LED



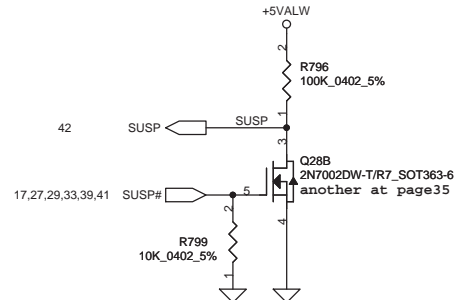
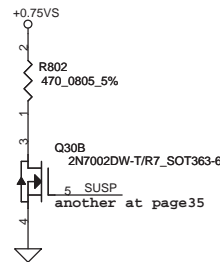
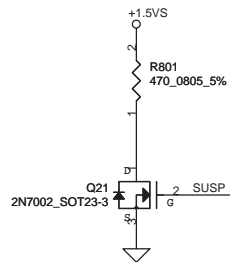
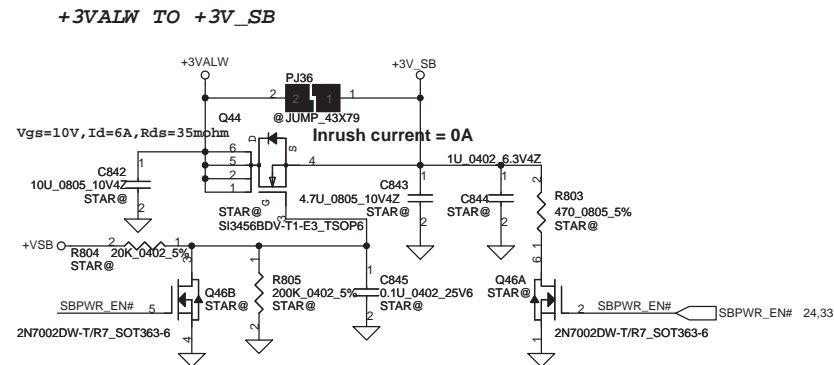
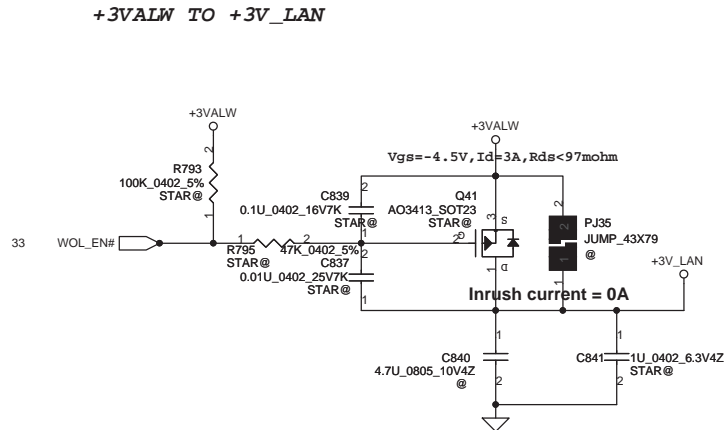
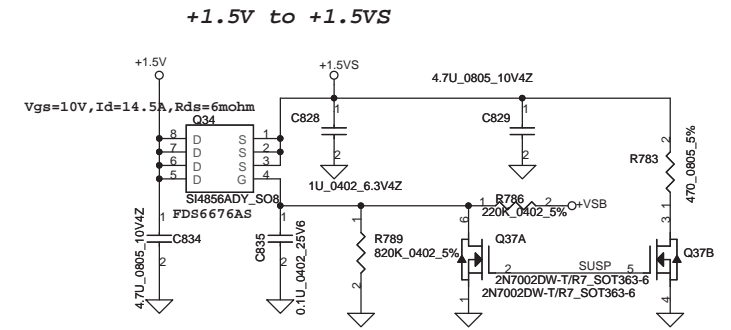
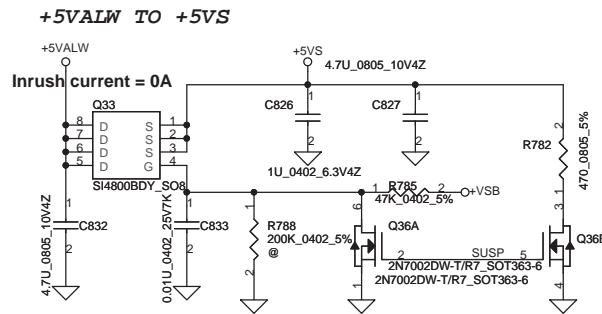
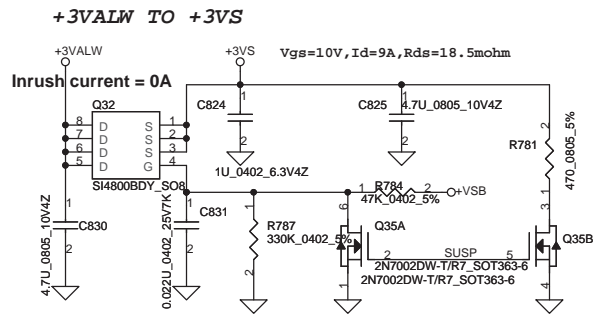
Screw Hole



PCB Fedical Mark PAD

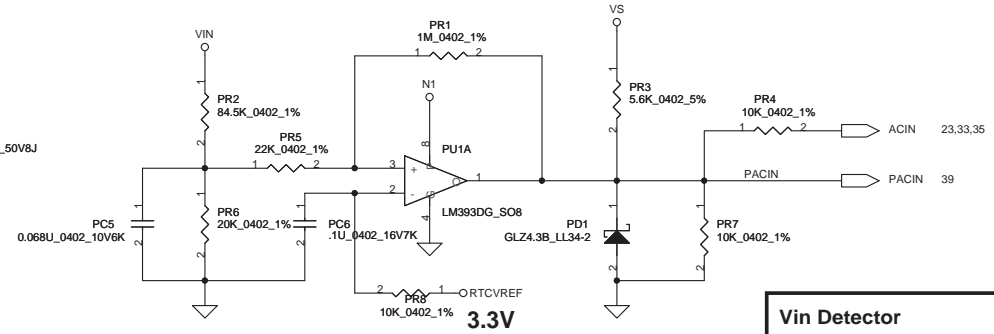
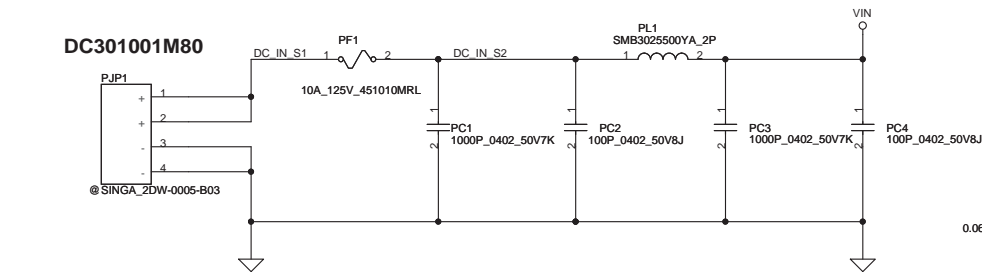


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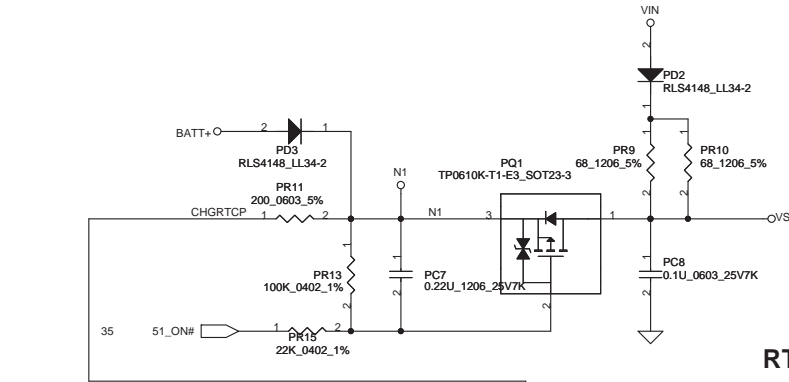
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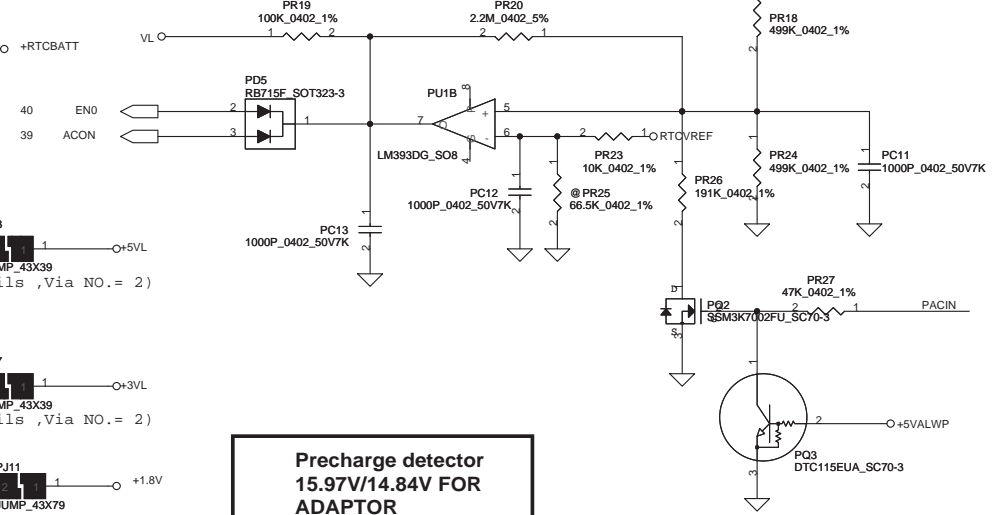
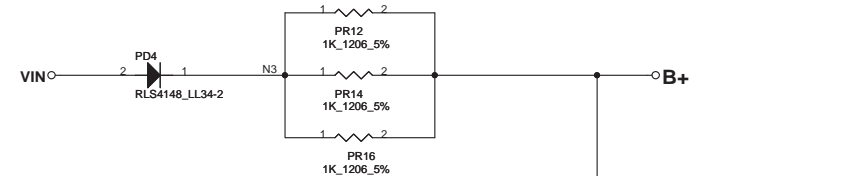
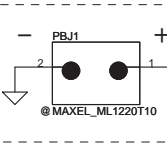


Vin Detector

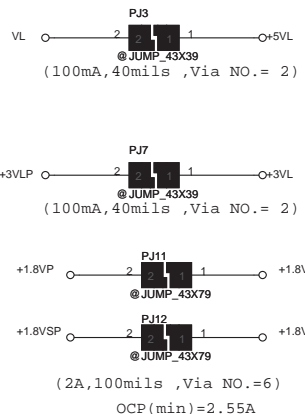
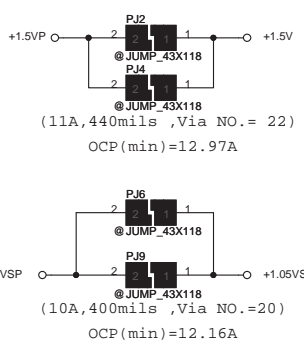
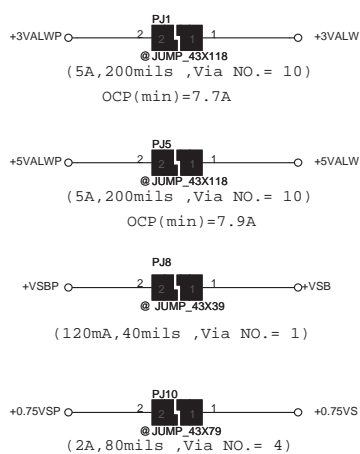
High 18.384 17.901 17.430
Low 17.728 17.257 16.976



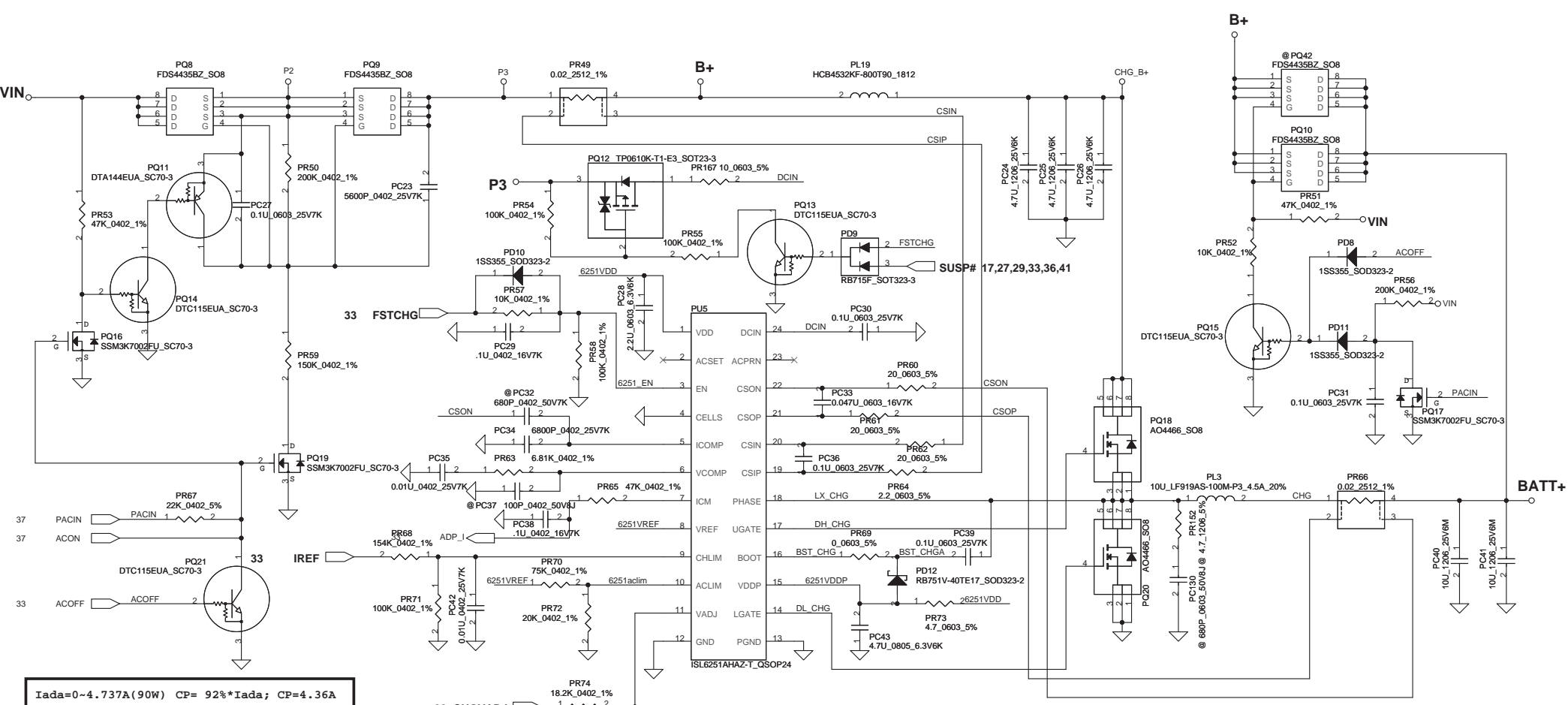
RTC Battery



Precharge detector 15.97V/14.84V FOR ADAPTOR



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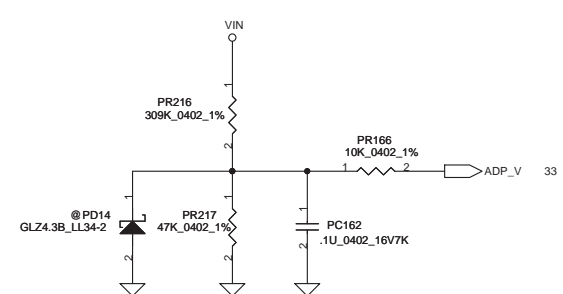
I_{ada}=0~4.737A(90W) CP= 92%*I_{ada}; CP=4.36A
I_{ada}=0~3.947A(75W) CP= 92%*I_{ada}; CP=3.63A
I_{ada}=0~3.42A(65W) CP= 92%*I_{ada}; CP=3.147A

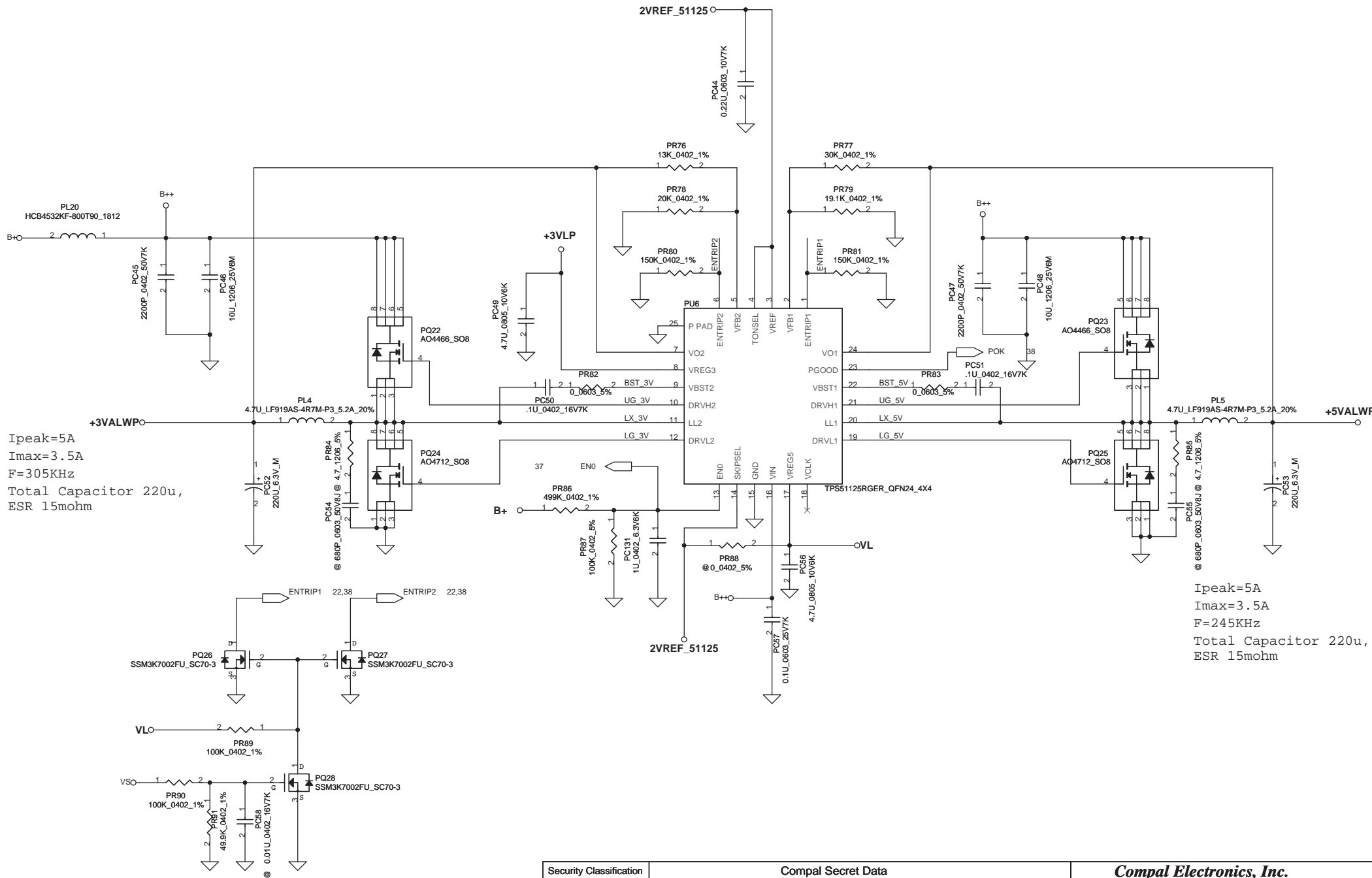
CP mode
V_{ac}lim=0.736V(90W) PR70=53.6k PR49=0.015
V_{ac}lim=1.08V(75W) PR70=24.9k PR49=0.02
V_{ac}lim=1.08V(65W) PR70=75k PR49=0.02

CC=0.25A-3A
I_{REF}=1.016*I_{charge}
I_{REF}=0.254V~3.048V
V_{CHLIM} need over 95mV

CHGVADJ=(V _{cell} -4)/0.10627	
V _{cell}	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CELLS	VDD	GND	Float
CELL number	4	3	2

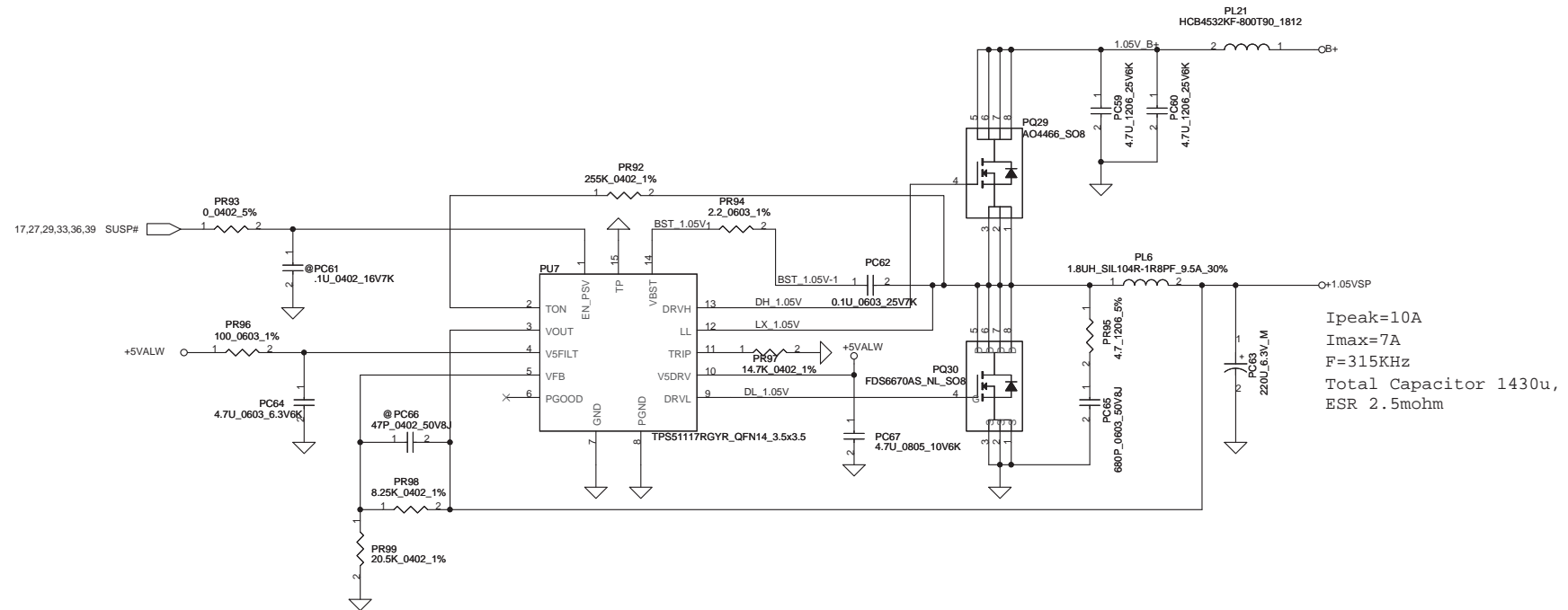




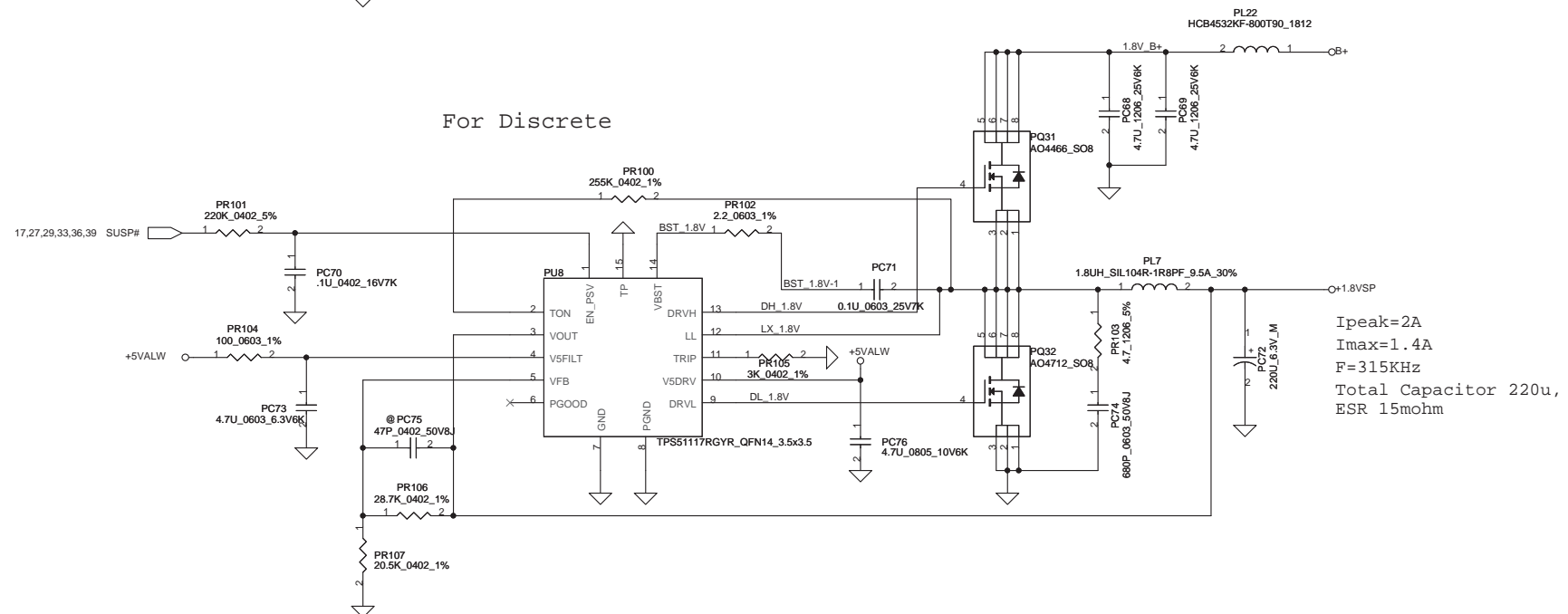
Ipeak=5A
Imax=3.5A
F=305KHz
Total Capacitor 220u,
ESR 15mohm

Ipeak=5A
Imax=3.5A
F=245KHz
Total Capacitor 220u,
ESR 15mohm

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For Discrete



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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT		P42-+CPU_CORE	change PU11 ISL6262 to ISL6266 Change PR145 6.81k to 8.25k Change PC112 470P to 270P Change PC114 220P to 100P Change PC116 1000P to 2200P Change PR155 255 to 100 Change PC118 0.018U to 330P Change PC119 0.018U to 330P Change PC120 0.018U to 0.01U Change upop component PC96 to PC97	change CPU_CORE IC modify the parameter for ISL6266
EVT		P40-1.05V/1.5V	Change PR97 13.7k to 14.7k	Modify trip resistor for ocp
EVT		P41-1.8VP/0.9VSP	Change PR112 15.4k to 18k	Modify trip resistor for ocp
EVT		P38-CHARGER	Add PC162 0.1U Add PR216 309k Add PR217 47k Add PD14 GLZ4.3B	Add detect adapter function
EVT		P38-CHARGER	Change PR49 0.02 to 0.015 Change PR70 24k to 53.6k Change PQ8,PQ9,PQ10,PQ42 FDS4435 to AO4407A Change PR69 2.2 to 0	Set CP for 90W(X6366051L02) For 90W(X6366051L02)
EVT		P38-CHARGER	Change PR70 24k to 24.9k	Set CP for 75W(X6366051L01)
DVT		P36-DCIN/DECTOR	Delete PD13 ENTRIP1 signal change to EN0 ENTRIP2 signal change to ACON Change PR23 34k to 10k Add @ lable to PR25 66.5k	Precharge detector circuit modify
DVT		P39-3VALWP/5VALWP	Add EN0 signal from PU6 pin 13	Precharge detector circuit modify
DVT		P38-CHARGER	Change PR70 24k to 75k	Set CP for 65W(X6366051L03)
DVT		P42-+CPU_CORE	Add PC126,PC127,PC128,PC129 330PF Add PR134,PR146 4.7 ohm Add PC102,PC111 680PF Change PR140,PR144 0ohm to 2.2ohm	For EMI solution
DVT		P38-CHARGER	Change PR71 100k to 120k Change PL3 16U to 10U	Modify charging current for 12 cell
DVT		P42-+CPU_CORE	Change PR145 8.25k to 11.3k	Modify switching frequency
PVT		P38-CHARGER	Change PL3 Part NO SH000003080 to SH162100M10	SH000003080 footprint is wrong
PVT		P36-DCIN/DECTOR	Change PU1 8 pin connect to N1	For precharge function
PVT		P38-CHARGER	Add PR166 10k Ohm	Modify ADP_V circuit(2009/02/18)
PVT		P38-CHARGER	Remove PD14	Modify ADP_V circuit(2009/02/18)
PVT		P38-CHARGER	Change PR74 18.2k to 15.4k	Change CHGVADJ voltage dividers value(2009/02/18)
PVT		P42-+CPU_CORE	Change PC126,PC127,PC128,PC129 (SE068331K80) to (SE00000FD80)	Change temperature tolerance K(10%) to J(5%)(2009/02/23)
PREMP		P38-CHARGER	Add PR167 10_0603_5%	Add 10 Ohm to DCIN circuit(2009/03/12)
PREMP		P38-CHARGER	Add PL19 HCB4532KF-800T90_1812 and delete PJ12	Add bead on B+ node(2009/03/12)
PREMP		P39-3VALWP/5VALWP	Add PL20 HCB4532KF-800T90_1812 and delete PJ13	Add bead on B+ node(2009/03/12)
PREMP		P40-1.05V/1.5V	Add PL21 HCB4532KF-800T90_1812 and delete PJ14 Add PL22 HCB4532KF-800T90_1812 and delete PJ15	Add bead on B+ node(2009/03/12) Add bead on B+ node(2009/03/12)
PREMP		P41-1.8VP/0.9VSP	Add PL23 HCB4532KF-800T90_1812 and delete PJ16	Add bead on B+ node(2009/03/12)
PREMP		P39-3VALWP/5VALWP	Change PR79 19.6k to 19.1k	Modify 5V to 5.14V(2009/04/08)
PREMP		P38-CHARGER	Change PR65 100 to 47k	For CPU throttling setting(2009/04/08)
PREMP			Change PR82,PR83,PR94,PR102,PR110 SD014000080 (0 +-1% 0603) to SD013000080 (0 +-5% 0603)	Component not haven 0_+~1%, change to 0_5%(2009/04/08)
PREMP		P42-+CPU_CORE	Change PC126,PC127,PC128,PC129 (SE0000FD80) to (SE074331K80)	Change property NPO to X7R(2009/04/08)
PREMP		P41-1.05VSP/1.8VP	Change PR96 422 ohm to 100 ohm Change PC64 1U to 4.7U	Avoid 2nd source RT8209B can not power on(2009/07/27)
PREMP		P42-1.5VP/0.75VSP	Change PR111 422 ohm to 100 ohm Change PC82 1U to 4.7U	Avoid 2nd source RT8209B can not power on(2009/07/27)
PREMP		P42-1.5VP/0.75VSP	Change PR112 14.7k to 3.9k	Set 1.5V OCP to 13.25A(2009/07/27)
PREMP		P40-3VALWP/5VALWP	Change PC52, PC53 SF22001M200 to SF000001H00	SF22001M200 is forbids to use (2009/08/04)
PREMP		P41-1.05VSP/1.8VP	Change PC63, PC72 SF22001M200 to SF000001H00	SF22001M200 is forbids to use (2009/08/04)
PREMP		P42-1.5VP/0.75VSP	Change PC81 SF22001M200 to SF000001H00	SF22001M200 is forbids to use (2009/08/04)
MP		P42-1.5VP/0.75VP	Change High,Low side Mosfet and Choke. Add bead on B+ node	(2009/06/18)
MP		P38-BATTERY CONN / OTP	Change PR33 13.7k to 12.4k Change PR37 15.4k to 15.8k	Change resistor for OTP (2009/09/01)

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PIR (Product Improve Record)

KSWAA LA-4982P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	7/22	15	delete C604-C610,C643-C645	Change reference plane of control from VCC to GND
2	7/24	35	change PCB P/N to DAZ07300200	For load BOM
3	7/27	14	add CD45 and un-mount CD17,CD39 on DDR 1.5V	design change

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